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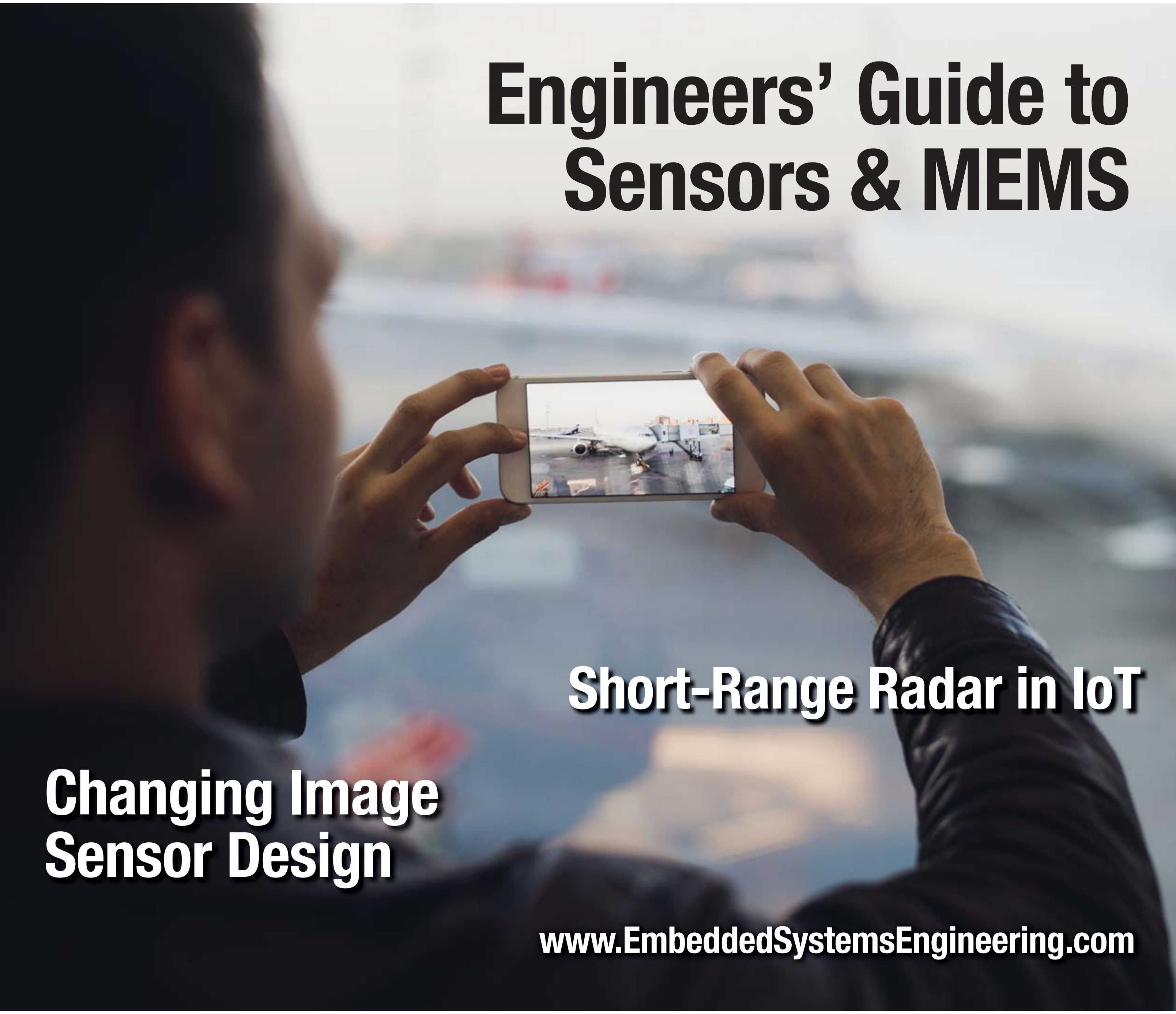

Engineers' Guide to Sensors & MEMS

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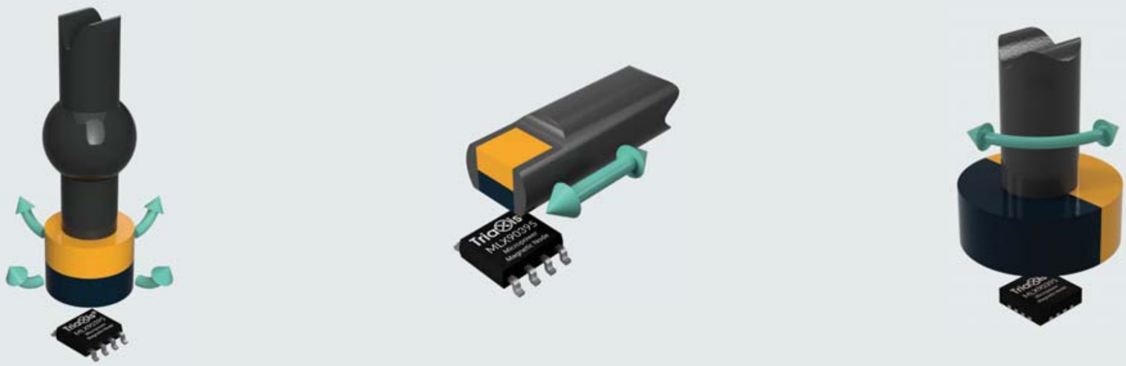

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Technologic Systems

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Developing MEMS for Volume Manufacturing, Part One

What methodologies and best practices bring about effective commercialization of a MEMS device?

By Alissa M. Fitzgerald, Keith M. Jackson, Charles C. Chung, and Carolyn D. White

Editor's Note: In the first of a three-part series, the authors survey the MEMS volume manufacturing landscape, introduce the concept of translational engineering, and name four characteristics a prototype must possess to show manufacturing readiness. The second article in the series will cover designing for testing and data gathering as well as for package and system integration, with the concluding article offering guidance on fabrication of advanced prototypes and on the process of transfer to the foundry.

Adapted with permission from Translational Engineering: Best Practices in Developing MEMS for Volume Manufacturing.[1]

FROM RESEARCH PROJECT TO COMMERCIAL PRODUCT

Aiming to advance technology and knowledge, academics invent MEMS devices. When market opportunities appear, a new goal arises: commercializing the technology. However, the initial prototype was never engineered to meet this new goal. Before a new MEMS device can be commercialized, it must be reengineered and adapted for the volume manufacturing environment. We address these reengineering and volume manufacturing issues by introducing "translational engineering," a method we developed over the past 15 years and more than 160 client projects.

Many new MEMS devices, whether sensors, actuators, or passive microstructures, are invented and initially developed in a university or a government-sponsored laboratory. In that setting, researchers focus on demonstrating new physics of operation or enhancing performance capabilities using new materials and methods. Then comes the first "proof of concept" prototype. The researchers create these prototypes using the tools available within their own laboratory, typically much older models that have been donated or purchased used. Often, because of limited equipment or budget, manual fabrication steps may be used. In a research project, a successful prototype is defined as one that provides sufficient insights and data for the publication of a peer-reviewed journal article, so these fabrication limitations are acceptable.

MEMS (or semiconductor device) research often inspires entrepreneurial ambitions, and many new companies have been formed on the basis of a founder's Ph.D. dissertation. However, one cannot simply send a successful research prototype straight to a foundry for commercial manufacturing. A research prototype developed solely for academic purposes has several deficiencies for commercial manufacturing:

1. The relationship between process tolerances and device performance is not yet fully understood.

2. The process may involve the use of machines, materials, or methods not commonly available in production facilities.

3. The design and process have not yet been optimized for items crucial to a commercial product, that is, packaging, testing, high yield, and low cost.

Successfully commercializing technology created in a research environment requires specially focused development work. Sometimes referred to as "design for manufacture," this effort is one we call "translational engineering," because the original intent of the inventors must be interpreted and translated into a design that can be manufactured in volume (thousands to millions or billions of units per year). This work is needed for MEMS especially because the design and fabrication process of a MEMS device are heavily interdependent. Small design changes will impact the process flow and vice versa. Depending on the complexity of the device design and its process, translational engineering can span years and consume millions of dollars before commercial production can begin. It is a necessary and unavoidable step in MEMS development. Many MEMS startups have failed because developers and other stakeholders substantially underestimated the time and funds that translational engineering demands.

MANUFACTURING ENVIRONMENT ECONOMICS

The goal of translational engineering is to deliver a MEMS design and process flow to a production fab for manufacturing. To sharply focus such development efforts, one must first understand and appreciate the volume manufacturing environment.

[1] *Sensors and Materials, Vol. 30, No. 4 (2018) 779-789 MYU Tokyo*

Wafer fabrication facilities ("fabs") are complex factories whose construction costs a minimum of $100 million for MEMS production and a minimum of $2 billion for state-of-the-art semiconductor production. These costs, and significant recurring operating costs, can only be justified by operations focused on high manufacturing throughput, 24/7 operation, and equipment utilization rates as close to 100% as possible.

Foundries (contract manufacturing fabs) therefore seek customers who will buy large quantities of wafers per year. Minimum order quantities of 5,000 wafers per year are common for high-volume MEMS foundries producing 200-mm-diameter wafers. Even smaller foundries, producing 150-mm-diameter wafers, may require minimum order quantities of 500 wafers per year, with 100 wafers per year being a typical minimum.

Fabs typically run dozens of different products. In some cases, fabs run both CMOS (semiconductor) and MEMS products, each of which have distinct process flows, through the same facility. Managing so many groups of wafers moving along different paths through the fab and keeping the tool utilization high require complex and detailed tool scheduling. Each tool will have a queue of wafer batches waiting their turn. Disruption of that queue or the tool (for example, to conduct experiments) will cause cascading schedule problems. Owing to this complex operating environment, fabs strongly favor producing MEMS that will be compatible with their existing tools and processes.

The foundry business model demands the selection of customers having the lowest risk processes at the highest possible profit margin in order to derive the most profit possible from the fixed production capacity of a facility. While a foundry might consider, for strategic reasons, accepting a customer with a new type of design or process, the foundry will very likely charge higher prices to compensate for the anticipated disruptions to its existing operations. Any development work undertaken by the foundry requires special attention from foundry engineers, which will be charged to the customer (as nonrecurring engineering fees). The foundry will also want to retain rights to any new process intellectual property (IP) developed. If a customer's process is deemed too early stage or too different from core processes, the foundry will likely decline the business outright.

With an understanding of the foundry business model just described, one can better appreciate that a proof-of-concept prototype is too fragile to go straight to a production facility. The translational engineering work to be carried out must be focused on ruggedizing the technology for the demanding production environment; the MEMS design and process flow must be engineered to require a minimum of human intervention during fabrication, have process tolerances that are comfortably met by existing fab equipment, and for each process step, have well-defined pass/fail criteria, which can be easily inspected using common metrology equipment.

In summary, a totally new prototype must be designed and built. This advanced prototype is what will eventually be transferred to a foundry for production.

Preparing for Manufacturing

The advanced prototype demonstrates readiness for manufacturing. In addition to the functionality demonstrated by the earlier proof-of-concept prototype, an advanced prototype must also have the following new attributes.

- A model of how process tolerances affect device performance
- A process flow and mask layout that can be executed in a production fab
- A design that considers downstream packaging, testing, and system integration needs
- A fabrication cost that allows adequate profit when sold in a given market

DESIGNING ADVANCED PROTOTYPES

Developing Parameter Sensitivity Models

A device technology is not fully mature nor manufacturable until one understands how all process parameters contribute to its proper function. In other words, how sensitive is the device performance to variation in each process step? Knowing the parameter sensitivities enables both implementation of inspection on that process step and establishment of pass/fail criteria to screen out wafers whose process variations will cause device failure.

For example, film thickness is one of several parameters that affect the stiffness of a membrane device and its resonant frequency. How thick or thin could that film be before the variation in stiffness impairs overall device performance? Membrane stiffness is proportional to the cube of film thickness. If the required device performance depends on controlling membrane stiffness to within ±10%, then the film thickness must be controlled to within +3.2and –3.5% (the cube roots of 1.1 and 0.9, respectively). If a deposition tool cannot repeatedly perform within those thickness tolerances, then the process will depend on luck (random variable) to achieve the correct film thickness and will therefore have poor yield.

Exploring and understanding parameter sensitivities is best done using simulation. The simulation environment allows one to explore the interaction of many design parameters much faster and more cost effectively than by building and measuring actual devices.

First, an adequate model of the device physics must be created. The model does not require precise material properties data nor does it need to look exactly like the finished device; it must, however, capture the fundamental physical behaviors of the device. At this stage of the development, we seek to understand how relative changes in input variables affect device performance, not to calculate absolute values with precision.

Often, a lumped parameter model (such as the equations for a mass-spring-damper system) is sufficient to elucidate the sensitivity to major process variables. Such a model could be implemented on an Excel spreadsheet or a Matlab script and used to quickly identify the most sensitive parameters and their approximate range of acceptable tolerances. Once first-order behaviors and sensitivities are well understood, then a more advanced model could be created by finite element analysis (FEA) simulation to study the subtler parameter interactions. For example, FEA is well suited to explore interactions with 3D geometries. FEA models can be time-consuming to build and verify, so engineering judgment must always be applied to determine the appropriate level of detail in a model. The ideal FEA model contains only enough features to correctly simulate the critical physical behavior and no more.

Data and insights gained from parameter sensitivity modeling must inform process integration and design layout. Typically, several iterations are needed between modeling and process integration before convergence to an advanced prototype design.

Process Integration and Mask Layout for Manufacturing

Designing an advanced prototype requires creating a process and mask layout that can eventually be executed by a production fab. The following factors are important when translating a proof-of-concept design.

- Selecting processes compatible with those at production fabs
- Engineering the device design to function within reasonable process tolerances
- Having clear prototype performance goals in order to guide process and design trade-offs

For smooth commercialization, it is essential to create an advanced prototype using processes commonly found in production fabs. Any chemicals, photoresists, or tools needed for the process must already be commercially available. Processes should not require individual wafer-by-wafer tuning, nor any manual steps. All materials and chemicals must be compatible with the types of foundries to which the product could eventually be transferred. For example, if the likely manufacturer will be a CMOS foundry, then materials such as gold or processes such as KOH etching, both of which contaminate CMOS devices, cannot be used.

Even with processing of very large volumes of wafers under stable conditions, all manufacturing processes have some random variation that will cause a plus or minus tolerance on dimensions and material properties. An advanced prototype design must be engineered to work within the limitations of available processes. This requires a deep understanding of how typical manufacturing processes perform and then creating a design that can accommodate those process imperfections. Creating designs that can succeed within typical process tolerances will maximize the selection of candidate foundries, which in turn will help get competitive pricing for volume manufacturing.

When developing an advanced prototype, the goal should not be perfect performance but making sure the device will function. There might be one step where tight process tolerances may be required, but it is always worth considering if sacrificing a certain performance will allow a wider tolerance and therefore a higher overall chance of creating a working device. Test data from an imperfect device is useful for tuning the models and the design as well as for identifying further process optimization. A second, subsequent prototype could always be used to further improve the design and process. The opportunity to learn is greatly diminished if a prototype fails to demonstrate even basic functionality.

Interactions and tolerances between the registration of different mask layers must also be carefully considered. The results of this analysis will eventually help to establish design rules for future device design. Minimum linewidth or spacing between the features on each layer is defined by the lithography variation and etch accuracy. The minimum overlap or spacing required between layers is defined by a combination of lithography variation and layer-to-layer alignment accuracy of the exposure tool.

Typically, misalignment errors and lithography variations are considered to be normally distributed random errors. This enables one to calculate an overall expected error from accumulated tolerances by adding the sum of the squares of each contributing error and then taking the square root. An advanced prototype's layout should reflect a realistic lithography error "budget."

In MEMS, process and design are inseparable. While considering trade-offs between the two, the big picture in business and technical goals must always guide engineering choices. Whether the technology is being commercialized by a startup company or a Fortune 500 company, prototypes must always demonstrate capability in order to be further funded. As different processes or designs or layouts are considered, they should be evaluated and guided by the goals of what the prototype must eventually demonstrate. Choices should always be conservatively made to ensure that it will be possible to yield some working prototypes, even if they have less-than-ideal performance. An overly ambitious, high-risk prototype that is designed idealistically for a perfect outcome but ultimately fails to work in practice is much less useful.

The authors are employed by A.M. Fitzgerald & Associates, LLC (www.amfitzgerald.com), a MEMS product development company located in Burlingame, CA, USA. Corresponding author email: amf@amfitzgerald.com.

New MIPI Camera Command Set Changes Image Sensor Design

Recent developments are making the process of integrating image sensors into devices across industrial, consumer, security and automotive markets faster and easier.

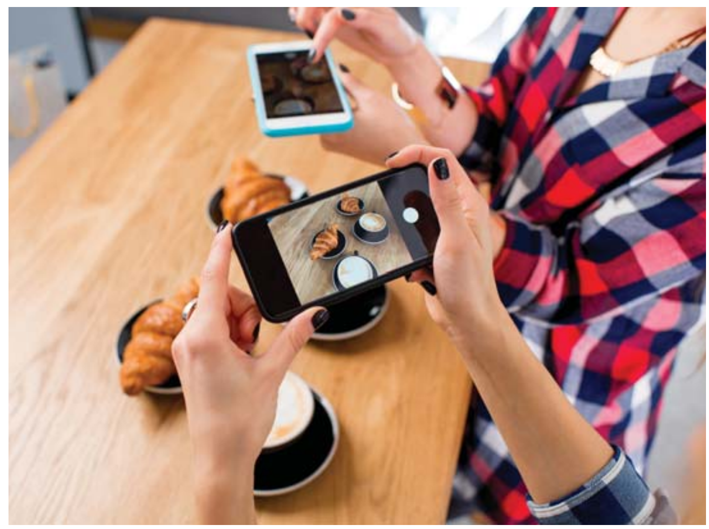
By Mikko Muukki, MIPI Alliance

Try to find a new connected device that doesn't have at least one embedded camera. You probably can't. The number of image sensors in smartphones, film cameras, digital still cameras (DSCs), digital single-lens reflex cameras (DSLRs), and mirrorless cameras alone has grown from 100 million worldwide in 2004 to 1.5 billion in 2016, according to the Camera and Imaging Products Association (CIPA).

The universe of devices using image sensors has ballooned, now comprising applications from casual to biometrics to connected cars to factory automation and more.

That proliferation is because image sensors are increasingly used for more than just taking photos and videos. For example, in IoT devices, image sensors sometimes are used for biometric authentication such as facial and iris recognition. And in connected cars, image sensors enable semi-autonomous driving and safety features such as collision-avoidance systems.

Those are just a few examples of how image sensors are now key for enabling market-differentiating and revenue-generating features in a wide variety of devices. As a result, device manufacturers and their suppliers need a way to quickly and cost-effectively integrate image sensors into their products.



That's why in November 2017, MIPI Alliance released Camera Command Set v1.0 (MIPI CCS v1.0), which significantly streamlines the process of integrating image sensors. The specification is designed for use by any company—including those that aren't MIPI Alliance members—in any device for any imaging application, from photography to video to machine vision. Here's an overview of the specification's key features and benefits.

FLEXIBILITY AND REPEATABILITY HELP REDUCE DEVELOPMENT COSTS AND LEAD TIME

MIPI CCS is a complete command set that covers a variety of basic and advanced features, such as resolution, frame rate, phase detection autofocus (PDAF), single-frame HDR and fast bracketing. Developers can use the specification to create a common software driver that configures the basic functionalities of any off-the-shelf image sensor that's compliant with both MIPI CCS and MIPI Camera Serial Interface 2 v2.0 (MIPI CSI-2 v2.0).

MIPI CSI-2 is the world's most widely used hardware interface for deploying camera and imaging components in mobile devices. MIPI CCS builds on that popularity and further increases interoperability, which helps to streamline integration and reduce costs for complex imaging and vision systems. All of that helps device manufacturers and their suppliers improve their products' competitiveness, profitability, and time to market. MIPI CCS provides:

- Mandatory controls for all relevant basic functions
- Identification
- Capability information to detect supported features and limits for system parameterization
- Embedded data for sync of sensor and host, such as 3A functionality
- Parameter retiming rules for robust operation so the host can understand better how the sensor behaves in certain conditions
- A standard register map

MIPI CCS specifies image sensor functionality at the register level. It's independent from the device's operating system and host system features, uses software drivers and only minimally specifies link-related items, thus enabling modular design principles. The net result is an architecture that gives developers the flexibility to use their MIPI CCS-enabled designs across multiple products. That's also an example of how MIPI CCS enables repeatable designs, which can reduce development costs and lead time for multiple products in a company's portfolio.

Figure 1 illustrates how MIPI CCS fits into a typical camera system. The system on chip (SoC) communicates with the image sensor over two paths. On the left is a bidirectional control link that uses MIPI CSI-2's Camera Control Interface (CCI), with the payload defined in MIPI CCS. The right link goes from the sensor's transmitter to the SoC's receiver and uses MIPI CSI-2 over MIPI D-PHY/C-PHY. This link carries data in formats defined in CSI-2, as well as metadata defined in CCS.

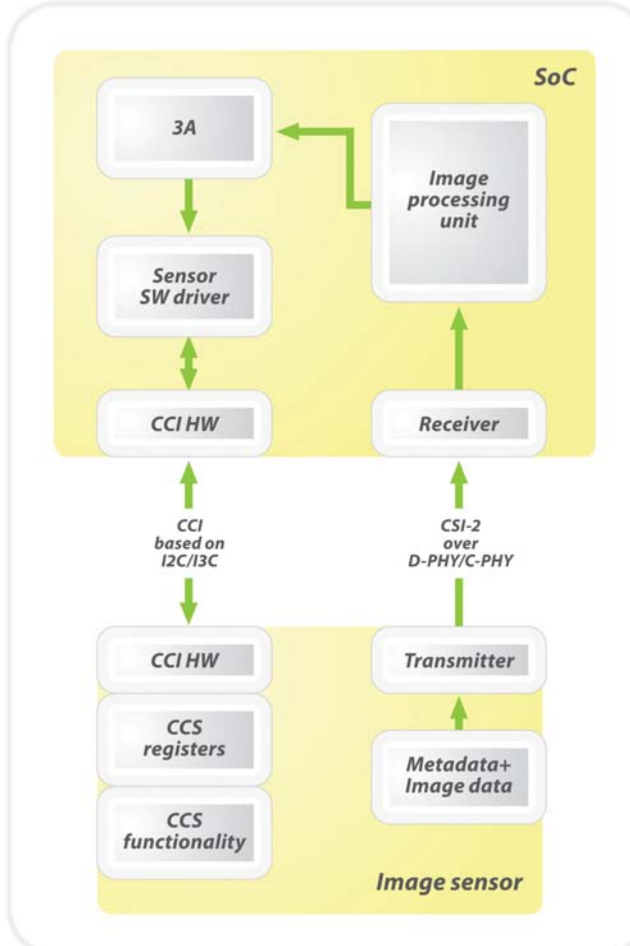


Figure 1: Typical Camera System with CCS

POWER UP, IDENTIFICATION AND DATA FORMATS

Using MIPI CCS, the software follows a sequence to power up and identify the camera module. This architecture gives developers flexibility when the image sensor shares a power supply with other modules.

Developers and manufacturers, including those that aren't MIPI Alliance members, can request an ID from http://mid.mipi.org. The identification process includes version control information for software parameterization, as well as binary capability information (e.g., whether a particular mode or feature is supported) and the limit values for software parameterization.

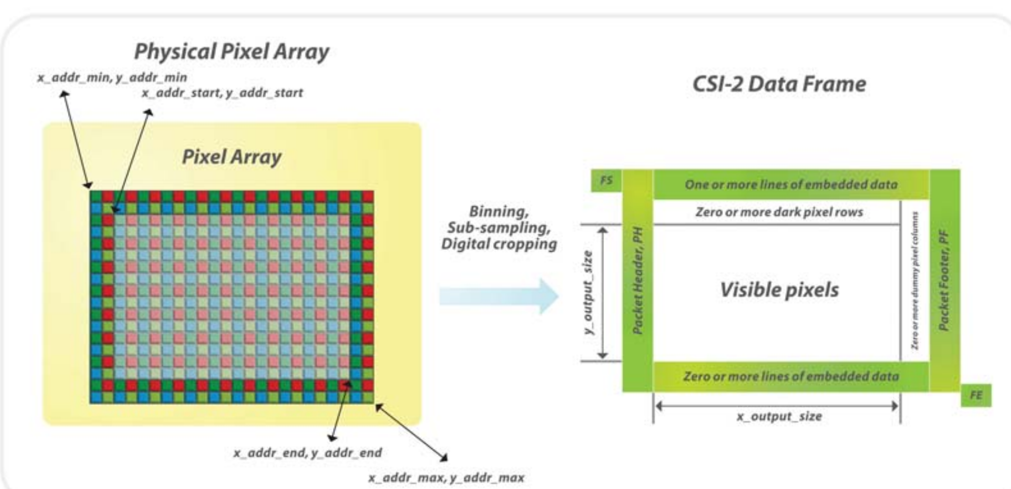


Figure 2: MIPI CCS Options for Changing the Resolution

MIPI CCS complements other MIPI specifications. For example, it supports all MIPI RAW and DPCM data formats defined in MIPI CSI-2 (v.2.0 and older) over D-PHY and C-PHY, such as RAW10 and DPCM10-8. Rather than defining the formats themselves, MIPI CCS defines the controls for selecting them. The CCI control interface, which can be based on I2C or MIPI I3C, provides access to standardized CCS registers and any additional manufacturer-specific registers.

RESOLUTION AND EXPOSURE PARAMETERS, EMBEDDED DATA

Developers have several options for changing the resolution with MIPI CCS, which covers the region of interest (analog, digital, and output crop) and readout mode (full, binning, and subsampling). To produce different resolutions, the pixel array can go through binning, subsampling, and digital cropping to produce the MIPI CSI-2 data frame, which consists of the visible pixels framed by a packet header and footer as shown in Figure 2.

MIPI CCS includes a variety of exposure parameters, starting with a mandatory set of basics that include the exposure time control and analog gain control. There's also an optional basic global digital gain control, while advanced options include single-frame HDR with timing and synthesis modes and fast bracketing.

The specification gives developers options for customization and market-differentiating innovation by supporting manufacturer-specific registers (MSRs). One example is using MSRs for global shutter, while CCS exposure controls handle rolling shutter.

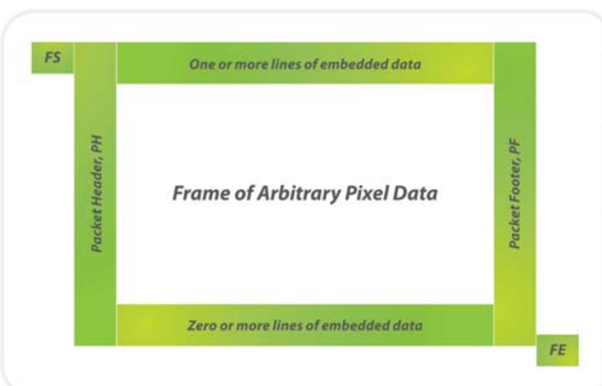


Figure 3: MIPI CCS Use of Embedded Data to Sync Host and Sensor

Embedded data can be used to synchronize the host and sensor. As Figure 3 shows, MIPI CSI-2 defines the embedded data at the top or bottom. Both are optional in MIPI CSI-2, but top is mandatory in MIPI CCS.

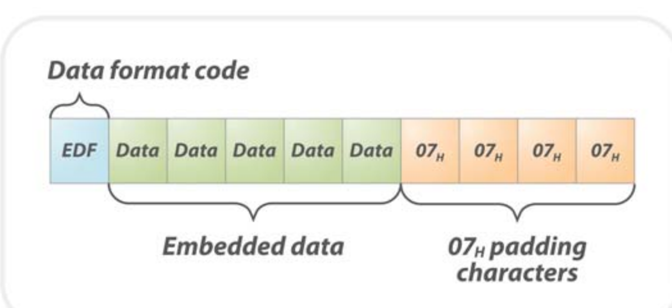


Figure 4: MIPI CCS Embedded Data Line Format

As Figure 4 shows, MIPI CCS defines the layer format for the embedded data lines, as well as the register information that must be transferred in the top line using a specific format. The specification also allows the use of the specific format for any MSRs and other camera command set registers in top-embedded data. Finally, MIPI CCS supports the use of other formats in additional embedded data lines.

PHASE DETECTION AUTO FOCUS, TEST MODES AND MORE

PDAF is an increasingly popular capability. MIPI CCS supports it by accommodating a variety of sensors:

- Those with only PDAF pixels
- Those able to separate PDAF pixels into different MIPI CSI-2 logical channel (virtual channel or DataType interleaving) from visible pixels
- Those with or without PDAF data processing

Finally, MIPI CCS specifies mandatory and optional test modes. These include programmable data, basic color bar, advanced color bar, and PN9.

ADDITIONAL RESOURCES

MIPI CCS includes a variety of additional features, such as frame timings and clocking, image correction controls, and an interface for sensor non-volatile memory. For detailed information about these features and more, download the specification.

More details may also be found in a recent webinar on MIPI CCS. Image sensor designers, software developers, camera engineers, and anyone who works with image sensors will benefit from the rapid integration of basic camera functionalities in a plug-and-play fashion without requiring any device-specific drivers.

Mikko Muukki is Expert, Imaging and Video Technology at Huawei. He has 14 years' experience in cameras and imaging, as well as additional experience in other technology fields. At MIPI Alliance, he is leading the MIPI CCS development.

Technologic Systems

TS-7553-V2 Single Board Computer

Compatible Operating Systems: Linux, Debian

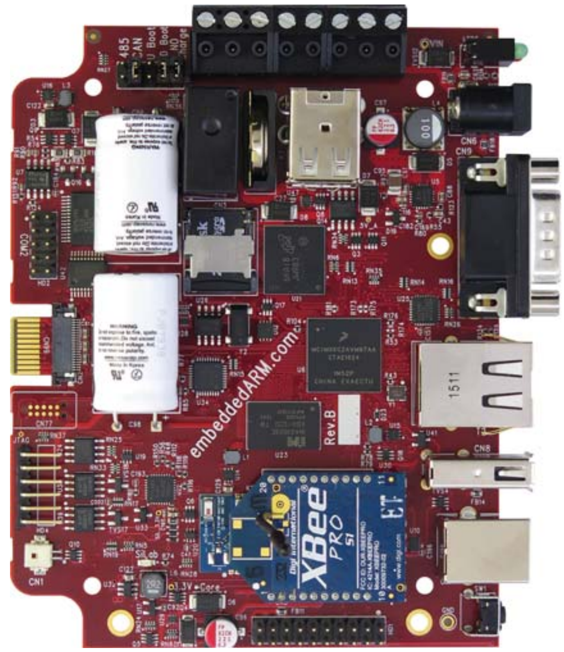
The TS-7553-V2 is developed around the NXP i.MX6 UltraLite, a high performance, ultra-efficient processor family featuring an advanced implementation of a single ARM Cortex-A7 core, which operates at speeds up to 696 MHz. While able to support a wide range of embedded applications, the TS-7553-V2 was specifically designed to target the Industrial Internet of Things (IIoT) sector. The TS-7553-V2 was designed with connectivity in mind. An on-board Xbee interface, capable of supporting Xbee or NimbleLink, provides a simple path to adding a variety of Wireless interfaces. An Xbee radio can be used to link in with a local 2.4GHz or sub 1 GHz mesh networks, allowing for gateway or node deployments. Digi and NimbleLink offer cellular radios for this socket, providing connectivity for applications such as remote equipment monitoring and control. Additionally, there is the option for a cellular modem via daughter card. Further radio expansion can be accomplished with the two internal USB interfaces (one on a standard USB Type A connector, and the second on simple pin headers). The USB interfaces enable support for multiple proprietary networks via a dongle or USB connected device. This provides the opportunity to run mesh, LoRa, ZigBee, automotive WiFi or other protocols with the TS-7553-V2 . All of these radio options, combined with the on-board 10/100Base-T Ethernet, create the opportunity to communicate seamlessly with up to five different networks simultaneously from a single point.

TS-7553-V2 Single board computer that features extensive I/O capabilities, low power consumption, and fanless operation over full industrial temperature range.

Product URL:
https://www.embeddedarm.com/products/TS-7553-V2

FEATURES

- NXP i.MX6UL 698MHz ARM Cortex-A7 CPU
- 512 MB DDR3 RAM
- 4 GB MLC eMMC Flash
- 4 USB ports (3 host interfaces and 1 device)
- Onboard WiFi and Bluetooth 4.0



TECHNICAL SPECS

- Nine-Axis Micro-Electro-Mechanical System (MEMS) motion tracking device containing a gyroscope, accelerometer and compass are optional on-board
- Fanless temperature range of -40°C t0 85°C
- Free extraordinary hardware and software support from the engineering team
- 10+ Year Guaranteed Lifecycle
- The TS-7553-V2 is the first Technologic Systems computer to offer Buildroot

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