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The High-Frequency Signals of PCIe 4.0 Demand Higher Performance from Engineers

PCI 4.0 meets growing throughput demands but requires hair-pulling attention to detail from engineers to make it happen.

By Lynnette Reese, Editor-in-Chief, Embedded Systems Engineering, Embedded Intel Solutions

If a processor has to access a peripheral, it might use Peripheral Component Interconnect Express (PCIe® or PCI Express®). PCIe is a high-speed serial computer expansion bus that replaced PCI (a parallel bus). PCIe, a dual simplex point-to-point serial connection, is a product of an Intel® R&D Lab begun in the 1990s. It briefly competed with a couple of other standards but gained momentum for broad adoption by the mid-'90s. The latest standard, PCIe 4.0, launched in October 2017, increasing speeds to 16 Gb/s per lane. This means that PCIe 4.0 is switching a voltage sixteen billion times per second over a differential pair.

“An acceptable eye height for PCIe 3.0 is 25 mv. For PCIe 4.0, it’s reduced to 15 mv.”

PCI Express is scalable, as well. PCIe 4.0 can be implemented as one lane up through sixteen bidirectional lanes, at almost 16 GT/s. Each lane is a differential pair comprised of one transmit signal and one receive signal. For more bandwidth, PCIe is commonly scaled up to two (x2), four (x4), eight (x8), or sixteen lanes (x16), although the standard allows up to 32 (x32) lanes. If there are 16 lanes of PCIe 4.0 in use, total throughput can reach almost 64 GB/s, with 16 signals transmitting and 16 signals receiving at the same time.

EVOLVING APPLICATIONS

PCIe has evolved to accommodate the need for speed in other technologies, such as storage. PCIe Express is most widely recognized for network cards and enabling gaming-level graphic cards. However, beginning with PCIe 3.0, it also began implementation for storage on Solid State Drives (SSD). SSDs are much faster than magnetic hard disk drives (HDDs), which have been in use since before conventional PCI was invented. SSDs found a distinct advantage in faster access through a PCIe serial bus standard. With PCIe, the SSD industry gained the advantage of speed. What’s more, the PCIe standard was already proven and demonstrated excellent interoperability with other products. Personal computers with an SSD may have a SATA or SATA Express connection, as they may be lower cost than PCIe. However, the SSD industry is starting to move to PCIe, most using an M.2 connector (previously known as Next Generation Form Factor). In addition to PCIe 3.0, the M.2 connector standard can also

Table 1: PCIe through the years. PCIe 4.0, when scaled up to 16 lanes, has a total throughput of 31.5 GB/s. *The term “GT/s” means Gigatransfers per second. “Transfers per second” includes overhead bits, which is more realistic, since bits per second would include overhead that does not contribute to throughput.

<table>
<thead>
<tr>
<th>Standard Version</th>
<th>Raw Bit Rate (GT/s)*</th>
<th>Throughput per lane (x1) in each direction</th>
<th>Total Bandwidth @ 16 lanes</th>
<th>Introduced</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe 1.0</td>
<td>2.5 GT/s</td>
<td>250 MB/s</td>
<td>8 GB/s</td>
<td>2003</td>
</tr>
<tr>
<td>PCIe 2.0</td>
<td>5 GT/s</td>
<td>500 MB/s</td>
<td>16 GB/s</td>
<td>2007</td>
</tr>
<tr>
<td>PCIe 3.0</td>
<td>8 GT/s</td>
<td>985 MB/s</td>
<td>~32 GB/s</td>
<td>2010</td>
</tr>
<tr>
<td>PCIe 4.0</td>
<td>16 GT/s</td>
<td>1,969 GB/s</td>
<td>~64 GB/s</td>
<td>2017</td>
</tr>
<tr>
<td>PCIe 5.0</td>
<td>32 GT/s</td>
<td>3,938 GB/s</td>
<td>~128 GB/s</td>
<td>~2019</td>
</tr>
</tbody>
</table>

*The term “GT/s” means Gigatransfers per second. “Transfers per second” includes overhead bits, which is more realistic, since bits per second would include overhead that does not contribute to throughput.

Figure 1: PCIe terminology. A differential signal is carried by a pair of wires, as differential signaling helps maintain signal integrity. Two of these differential pairs are in each lane; one pair to transmit and one pair to receive. A link describes the physical connection between PCIe devices regardless of the number of lanes. (Credit: Ravi Budruk, PCI Express Basics)
accommodate Serial ATA (SATA) 3.0, and USB 3.0 (backward compatible as USB 2.0). Although the SATA interface is well-established and widespread in the embedded space, PCIe for storage is growing in high-performance computing and other applications where load times are a concern. However, SATA is expected to coexist with PCIe in the industrial and embedded markets for several more years. Non-volatile Memory Express (NVMe) is a specification developed for SSDs that uses PCIe for data transfer. NVMe is employed more with SSDs of substantial capacity and is therefore used more in the server market rather than embedded applications. Most embedded applications typically do not require the huge, fast, and (presently) more costly storage of an SSD. However, PCIe’s reliability plays a good part in why PCIe is becoming the standard interface on the storage side.

One example of PCIe used in high-performance computing is in weather forecasting. Meteo-Swiss, the Swiss Federal Office for Meteorology and Climatology, uses servers densely populated with acceleration devices to compute weather forecast models for simulation. Meteo-Swiss achieves significant energy efficiency by connecting multiple accelerator devices (GPUs) using PCIe. Even so, PCIe networks must be engineered for a topology that reduces traffic congestion. A server or supercomputer that houses numerous accelerator devices (e.g., GPGPUs, Intel Xeon Phi) experiences an increased burden on intra-node communication networks using PCIe.

In the consumer market, PCI Express is used every single day, primarily with smartphones and tablets that use Thunderbolt™. Thunderbolt is a combination of PCI Express and DisplayPort into one standard, which of course we use to charge Apple products. According to Intel, Thunderbolt technology provides flexibility and simplicity by supporting both data (PCIe) and video (DisplayPort) on a single cable connection. “Thunderbolt™ 3 technology is 8x faster than USB 3.0 and provides 4x more video bandwidth than HDMI 1.4.” USB Type-C ports can also connect and communicate with Thunderbolt devices. Thunderbolt 3 uses four lanes of PCIe 3.0 and eight lanes of DisplayPort in one cable, with an integrated USB 3.1 (10 Gb/s) host controller. PCI Express is an excellent choice for mobile devices. The adaptable PCI Express has some very low power states, offers very high speed when it’s needed, yet barely sips power when it’s in a standby state. Some mobile devices internally use PCIe to drive data to and from the display or elsewhere.

HIGHER PERFORMANCE? HOW HIGH?
Whereas PCIe 3.0 was a radical departure from PCIe 2, the PCIe 4.0 protocol and encoding are similar to PCIe 3.0, as well as many other components. What makes PCIe 4.0 a challenge for the industry is that while throughput has increased dramatically with PCIe 4.0, the channels have not changed much from PCIe 3.0. The average channel length of a desktop computer is about 10 inches (~25 cm). Modern servers have channels measuring around 20 inches total. For PCIe 4.0 to increase in speed, higher frequencies must be put through the same channel that was used for the previous generation. However, the
tradeoff is an insertion loss, which is a loss that increases with higher frequencies. Insertion loss is a frequency-dependent loss in signal strength that is usually expressed in decibels. When you double the frequency, the result is a significant loss, and the ability to drive a signal into a channel and recover it at the other end is significantly diminished. PCIe 4.0 demands higher performance and considerably more attention to detail in implementation.

PCIe 3.0 survived in part because receivers have improved over the years. Using eye diagrams to test signal integrity, the acceptable level of eye height for an equalized PCIe 3.0 signal is 25 mV. For PCIe 4, that eye height has dropped to 15 mV.

Such a low voltage makes even a tiny level of noise an issue. Therefore, considerable attention to detail is going to be the means of implementing successful products, products that pass standards testing for PCIe 4, as well as interoperability testing with other PCIe 4.0 products. The PCIe 4.0 standard does specify a new component, a retimer, which takes data and passes it through as quickly as possible to allow you to extend the channel lane. A retimer has some advantages over a typical re-driver that relate to deterministic and random jitter. (Retimers were offered as an option in subsequent revisions to the original PCIe 3.0 standard). As Intel states it, “With PCI Express Gen4 (16 GT/s), data rate has increased by 2x compared to previous generation (8 GT/s), resulting in shorter channel reach. Common use cases include channels expanding over system boards, backplanes, cables, risers, and add-in cards.”

Another option to improve PCIe 4.0 performance is to use FR4 as the board material in printed circuit boards (PCBs). This approach mitigates frequency-dependent characteristics of the boards, which affects insertion loss to some degree. FR4 is fiberglass mesh that is weaved and pressed. Signal integrity issues are less of a problem with FR4 as a PCB material. Nevertheless, the signal integrity requirements of PCIe 4.0 are much higher than what engineers experienced with PCIe 3.0.

The PCIe 4.0 specification does provide guidelines for the new challenge it presents. PCIe is far from being “just an interface,” however. Phenomenal throughputs have been achieved with every release by PCI-SIG, the PCIe standards body, and thanks to the efforts of the multitude of engineers working to turn the specification into products that work well together. Successfully implementing the more demanding PCIe 4.0 will require not just adding a retimer, but also making small changes in many areas to accommodate high-frequency signals, from mounting connectors to meeting channel requirements for the specifications using statistical simulation. PCIe does not get as much attention as GPUs or processors that are tuned to implement neural networks, but without the significant gains the world has seen from PCIe in the past decade we could have been heading to yet another standard to create speed gains with an entirely different approach.

Lynnette Reese is Editor-in-Chief, Embedded Intel Solutions, and has been working in various roles as an electrical engineer for over two decades. She is interested in open source software and hardware, the maker movement, and in increasing the number of women working in STEM so she has a greater chance of talking about something other than football at the water cooler.
Q&A with Al Yanes, PCI-SIG

The first quarter of 2019 is on its way and so is the 1.0 version of PCI Express® (PCIe®) 5.0 specification.

By Anne Fisher, Managing Editor

Editor’s Note: The PCIe 5.0 Version 0.7 specification was released to members in June 2018. “5.0 primarily targets 400 Gigabit Ethernet and solutions that require doubling of the bandwidth without going wider,” PCI-SIG® President and Board Chair Al Yanes tells us. Edited excerpts of our interview follow.

EECatalog: PCI Express has that advantage of synergy because it is found in so many sectors.

Al Yanes, PCI-SIG: You hit the nail on the head. If you look at an embedded processor, it is going to use PCIe architecture; if you go to a mobile solution, you are going to have PCIe architecture. PCI Express technology is ubiquitous. For example, if you are designing a solution for enterprise, you may have picked it up on your previous assignment on storage for NVMe™.

“PCI-SIG® is focusing primarily on the speed change to accelerate our development of PCI Express® 5.0.”

You might realize, “I was working on storage for NVMe, and I have been moved to a mobile space and wanted to do an IoT solution—I can use PCI Express technology for that.” This is where the incumbent years of experience help; 20 million lines of code support the PCI Express

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Learn how you can use PCIe in your design
devices. It is a robust, solid, infrastructure from a tools perspective, from a software perspective, and from the perspective of debugging in the lab using oscilloscopes and logic analyzers, for example. PCI Express technology is very familiar and common, so the proliferation of that knowledge makes sense.

**EECatalog:** What are some of the market drivers for PCIe 4.0 and 5.0 architectures?

**Al Yanes, PCI-SIG:** Traditional enterprise servers as well as cloud storage via NVMe solutions. In the mobile space, we have seen increased adoption, primarily due to our L1 substates technology. L1 substates have a near zero idling power—this is something we introduced several years ago, and I have seen several of the mobile manufacturers adopt PCI Express technology, which is very good from a volume perspective.

**EECatalog:** Please give us a brief summary of the PCIe specification roadmap.

**Al Yanes, PCI-SIG:** The PCIe 4.0 specification came out in October 2017. We have completed the 0.7 version of the PCIe 5.0 specification, and we are projecting that the final spec will be available in the first quarter of 2019. The release of the PCIe 4.0 specification took seven years but on average we have been doubling bandwidth every three years. We are catching up with the PCIe 5.0 specification, which is anticipated to arrive in only two years.

The PCI Express 5.0 specification primarily targets 400 Gigabit Ethernet and solutions that require doubling of the bandwidth without going wider—where the only option they have is to go faster; we will remain the state of the art on bandwidth. If you do the math 400 GbE is 50 Gbps in each direction and a PCIe 5.0 x16 solution will give you 64 gigabytes in each direction for a total of 120 Gbps.

There is a lot of momentum already in the industry with 28 gig solutions and 56 gig solutions, so we are leveraging that. We are focusing primarily on the speed change to accelerate our development of PCIe 5.0 specification, even adjusting some of our specification processes to enhance development.

We believe PCI Express 5.0 architecture will continue to keep us at the forefront of interconnect technology with our members and with others who utilize PCIe architecture for their solutions. The PCIe 5.0 specification will meet the bandwidth needs across a range of industries like mobile, storage, 400 Gigabit Ethernet or Infiniband, accelerators and machine learning.

**EECatalog:** So PCI Express technology will be important for Artificial Intelligence, then?

**Al Yanes, PCI-SIG:** Yes, I was just reading the other day about Microsoft’s Project Catapult and those kinds of technologies are going to primarily utilize PCIe architecture based solutions.

At the Open Compute Project Summit, they emphasized 400 GbE; communication of data to their accelerators—all that is PCIe technology based. If you look at Microsoft’s Project Olympus—data is going to the GPUs via PCI Express architecture.

PCI Express technology is the main throughput for I/O into the CPU. Data going through PCIe. 5.0 technology will facilitate the machine learning, AI solutions and the accelerator attachments that Microsoft, Amazon and other heavy hitters are creating.
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TECHNICAL SPECS

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- **Speeds:** 2.5GT/s, 5GT/s and 8GT/s
- **Probes/Interposers:** active and passive PCIe slot, XMC, AMC, VPX, Express card, Express Module, Minicard, Mid-Bus, Multi-lead, External PCIe cable, CompactPCI Serial, U.2, M.2, OCuLink, and others
- **Form factor:** Card, Chassis

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- **Lanes supported:** x1, x2, x4, x8, x16
- **Speeds:** 2.5GT/s, 5GT/s, 8 GT/s, 16GT/s
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Protocol Tests

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  - Test NVMe Conformance (Required by UNH-IOL for NVMe Conformance Integrators List)
  - Corner Case Testing
  - LTSSM Testing
  - Dynamic Equalization Testing
  - Speed/link Test Arcs
  - G2 Validation tests
  - PTM Testing
  - L1 Substate Testing
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