Engineers’ Guide to FPGA & CPLD Solutions

Six Ways Synthesis Can Support Design Assurance in FPGAs

28nm—FPGAs Lead the Way in Semiconductor Innovation & Value

Bandwidth Demands Drive FPGA/PLD Market

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Welcome to the 2012 Engineers’ Guide to FPGA and CPLD Solutions

It’s an exciting time for engineers who are designing and developing with programmable logic devices. New technologies offer tremendous jumps in performance – along with complexity. As usual, we bring you insight directly from experts in the field to help you anticipate and address these new challenges.

Mentor Graphics shows “Six Ways Synthesis Can Support Design Assurance in FPGAs,” while Saelig Co. and Byte Paradigm explain “Working with Quad and Other SPI Protocols” and Loring Wirbel addresses verification tools in “FPGA Verification Must Address User Uncertainty for Prototyping, System Validation.” Jake Janovetz describes an evolutionary change in a particular FPGA application in “Machine Vision – Making the Leap from Frame Grabbers to FPGAs.” We also bring you the latest market and technology trends from Richard Wawrzyniak, senior analyst at Semico Research, in “Bandwidth Demands Drive FPGA/PLD Market.” Not surprisingly, our virtual roundtable discussion also focuses on new technologies; you won’t want to miss “Move to 28nm Brings Opportunities and Challenges.” And for more detail on this exciting advance, Xilinx offers some final thoughts in “28nm—FPGAs Lead the Way in Semiconductor Innovation & Value.”

Of course, that’s not all – this issue is full of product news, datasheets, events and other resources to keep you up to date with the latest in programmable logic. As always, we’d love to hear your feedback, thoughts and comments. Send them to info@extensionmedia.com.

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The FPGA market continues to be propelled by an insatiable demand for bandwidth in wireless networks, as well as the back-ends where those networks interface with wired networks. And that’s probably not going to change any time soon, says Richard Wawrzyniak, Semico senior market analyst for ASICs and SoCs, referring to aggressive forecasts for smartphone usage. He adds, “We haven’t even scratched the surface yet on video conferencing.” Wawrzyniak believes that the advent of reliable, useful and cost-effective video conferencing is likely to drive additional business usage that could push FPGA trends even higher. Key issues in how this plays out range from identifying viable revenue models to addressing cell phone battery life that currently gates talk time.

Barring additional dramatic hits to the world economic climate – which might change what consumers are willing to pay for mobile broadband access – Wawrzyniak doesn’t expect to see a slowdown in the FPGA market (see chart). Semico data shows that the total programmable market is close to $5.1 billion in 2011, with $4 billion of that coming from FPGAs.

“FPGA manufacturers have done a very good job of increasing performance and functionality, reducing costs and getting product out that is reasonable in power consumption,” he says. “Those were always the three areas where FPGA manufacturers faced the greatest challenges from the ASIC or SoC market: performance, cost and power.” Wawrzyniak cites the silicon interposer technology used in Xilinx’s new Virtex-7 product line as an example of an innovative new technology that should see extensive use; potentially not just in programmable logic. Xilinx uses 2.5D IC stacking to provide the capacity of four traditional monolithic FPGAs in a single 28-nanometer device, and at a fraction of the total power consumption.

Judging by recent product announcements from industry leaders Altera and Xilinx, CPU cores are an ongoing trend in FPGA development, as is the larger role that IP is playing in FPGA designs, whether the IP comes from the device manufacturer or from third parties. Wawrzyniak predicts a growing trend in IP subsystems from SoC designers in general, although at this point he says the trend is primarily limited to large companies that have developed those subsystems.
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The total programmable market is close to $5.1 billion in 2011, with $4 billion of that coming from FPGAs.

Internally, Wawrzyniak explains, “They’ve done it because they realized they need to do two things: one, reduce the level of effort that they’re expending to create very complex silicon and two, they want to move up a layer of abstraction.” As that trend plays out in the third-party market, it’s only natural that the approach designers use to prove out and test different kinds of IP will extend to FPGAs. Wawrzyniak adds, “One premise of IP subsystems is that they all have their own internal interconnects that the IP blocks that create the particular system-level function are arranged around. It’s logical that you would want to extend those interconnects from the subsystem out to the interconnects that are already on the device.”

While many FPGA manufacturers now refer to their devices as SoCs, that’s an evolution that’s occurred just over the past few years. Wawrzyniak doesn’t expect to see older architectures totally replaced by SoC architectures – they will coexist for a while – but he believes the handwriting is on the wall. Designers will continue to move in the direction that provides better performance along with greater complexity. And while development costs continue to climb, those increases aren’t due simply to more expensive IP and EDA tools: verification costs are huge, and time is money.

Cheryl Berglund Coupé is Editor of EECatalog.com. Her articles have appeared in EE Times, Electronic Business, Microsoft Embedded Review and Windows Developer’s Journal and she has developed presentations for the Embedded Systems Conference and ICSPAT. She has held a variety of production, technical marketing and writing positions within technology companies and agencies in the Northwest.
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With the large-scale integration of today’s systems-on-chips (SoCs), FPGAs can help embedded designers reduce cost, weight, area and power; they also offer flexibility so that designers can respond to new standards, evolving customer needs and other requirement changes and still meet their time-to-market window. But the complex architectures of these devices can also present new challenges to board-level designers. EECatalog talked to Matt Ferraro and Patrick Dietrich, Connect Tech hardware design engineers and FPGA specialists, about today’s FPGA-based designs and how to bring these boards to production more efficiently and cost-effectively, while addressing both current and future needs.

EECatalog: In what kinds of circumstances do developers typically need help with FPGA-based designs?

Ferraro: Connect Tech’s customers are generally those engineering teams that are knowledgeable, often engineers who have board-level design experience with general-purpose CPUs or microcontrollers, but only have experience using CPLDs as glue logic. They may lack experience using FPGAs or have limited resources recognizing that taking on a given project internally will jeopardize time to market.

Dietrich: Another typical situation is that experienced FPGA IP developers come to us once they’ve implemented their custom design in a development board, either from us or the FPGA vendor, but now want to bring their product to market. They may not have the experience or the resources to create the board-level design themselves. This is the ideal time to leverage our experienced FPGA developers, maintaining time to market as well as budgetary requirements.

EECatalog: When you start work on a new FPGA-based design, what are the first issues you address?

Dietrich: The first things we look at are the peripheral interfaces in the customer’s design that will be connected to the FPGA. Then we analyze each of these interconnects and determine their speed, interface, voltage level, I/O standards and how many pins are required. Another early issue we look at is estimating the actual FPGA design metrics. This leads to an indication of the logic density and speed grade needed from the FPGA, as well as clock rate and resource usage.

Patrick Dietrich: The latest-generation FPGAs often have built-in logic (or hard IP) to implement features such as Ethernet MACs, DDR memory, PCI Express (PCIe) endpoints, etc., so FPGAs are not only for glue logic like they were 10 years ago. Signals and interconnects have changed, clock frequencies are increasing and rise times are decreasing. A designer can no longer use any pin as a general-purpose I/O pin when designing with higher-speed signals – things like clocking resources and special transceivers are now grouped to specific pins or banks of pins.

Matt Ferraro: Today’s FPGAs are directly interfacing with all sorts of peripherals at high speeds, such as DDR3 memory, PCIe, SATA, HDMI/DVI, etc. Every peripheral has a different electrical interface standard, which has different voltage and timing requirements. To accommodate this, FPGAs have many special dual-purpose pins, such as voltage references, impedance references, I/O clock and strobes. Previous-generation FPGAs may have only had the global clock inputs, where every other pin is created equal – not unlike many of today’s CPLDs. The challenge now is to juggle all of these interface requirements in relation to the needs of the FPGA RTL design itself. You can’t afford to let the board design dictate the direction of the FPGA design or vice versa; both designs teams must work in concert to avoid rework in the design cycle.

EECatalog: What has changed in programmable logic that makes today’s board designs so complex?

Ferraro: Definitely, I/O interfaces are key. We ask a lot of questions to make sure we anticipate everything. What I/O standard are they using, and what’s the required voltage? How fast do they operate? What impedance is required? What’s the data rate? How many pins are required to support the
interface? What power is required by the peripheral, which comes into play later? Then as a parallel path, we need to analyze the FPGA RTL design itself. What are the internal clock rates? How many logic resources are required? Is any special hard IP required, such as DSP slices, Ethernet MACs or PCIe endpoints?

**EECatalog:** You mentioned power, which seems to be a bigger issue as more features and performance are integrated into new designs. Are there tricks to addressing power requirements?

**Dietrich:** From the early stages of the design, we create a power budget that defines the current required per voltage rail.
for the FPGA, which is based on I/O and resource estimates including logic usage, capacity usage, internal clock rates, I/O quantity, I/O data rates and I/O voltage levels. This can be difficult, because if you're used to dealing with microcontrollers and CPUs that have discrete power ratings, you'll notice that estimating power for FPGAs is very different and largely depends on what is being implemented in your design.

**Ferraro:** The next step is to create a power budget for the peripheral themselves, both on and off the board, and create a power tree, determining how each voltage rail is derived from the power input. All this is relatively straight-forward, but there are possible 'gotchas' that need to be considered. For example, are there any sequencing requirements for the FPGA, or sequencing requirements for the peripherals that conflict with the FPGA? Beyond inherent sequencing demands of the ICs, are there sequencing requirements for the design, such as certain ICs that need to be powered up before the FPGA or vice-versa? Or if there's no method to disable or idle a specific IC, is it necessary to delay its power-up until the FPGA is configured and ready?

**Dietrich:** We also need to determine how this will fit with on-board power supplies that might be present, which will also determine what additional supplies or power monitoring circuitry will be required on the PCB design.

**Ferraro:** Other questions we ask are things like whether there are voltage rails that need to be especially quiet. For example, perhaps the FPGA core voltage is 1.2V and the SERDES supply is also 1.2V; it might be necessary to isolate and drive the SERDES supply separate from the noisy core voltage. And we always want to consider the possibility of upgrading the capacity of the FPGA later in the same footprint, and whether the extra power requirement has been factored in.

**EECatalog:** Are there challenges around FPGA configuration that engineers need to be aware of?

**Ferraro:** Configuring a FPGA can be a trivial task, or it can be very complicated, depending on the application. Every design should have at a minimum a JTAG connection for debugging, development and production testing, as well as persistent storage for the application. The persistent storage is usually in the form of serial or parallel flash or a hybrid device produced by the FPGA vendor. In more complex designs, the FPGA could be configured by microcontroller, CPU, CPLD or other FPGA. But focusing on the flash design, there are quite a few things to consider. Are the flash configuration pins on the FPGA dual-purpose? Are these pins already tasked and connected to another device? If so, we need to make sure the I/O standards are compatible – flash is typically 3.3V CMOS. If the signals are shared, we need to know if the peripheral interface is high-speed; if so, it may not tolerate having another device in the signal path.

**Dietrich:** Sequencing requirements, such as the flash needing to be powered up a certain amount of time before it can be accessed by the FPGA, also need to be considered, as well as timing requirements, such as whether the FPGA can read data from the flash and configure itself in time. A perfect example is PCI and PCI Express, which specify that a device must be ready approximately 100 ms after power-on. For instance, we had a recent design of a PCIe software-defined radio peripheral card in which the FPGA had to read from the flash and be ready in less than 100 ms in time for the PCI configuration process.

**Ferraro:** And don't forget that many products need to be field-upgradeable over Ethernet or PCIe or USB, in order to add new features or fix bugs. In any of those cases, the designer has to consider whether the flash is writeable over the general I/O. Some FPGA vendor-specific flash is read only, and can only be written to via JTAG. And there are lots of other possible issues, such as whether the FPGA can restart the configuration cycle on the fly (a soft boot) without doing a power cycle (complete on/off), and whether the other circuitry can handle a temporary interruption in the state of the FPGA as it goes from configured to an un-configured state. Also think about what happens if the flash programming operation is interrupted; for example, if the Ethernet cable is disconnected. What if the flash is corrupt? In this case, consider designing a fail-safe configuration scheme where the first half of the flash contains a known good golden image and the second half contains the actual application image.

**EECatalog:** Once the board is ready for production, what approaches do you take to avoid expensive re-spins?

**Ferraro:** After all the FPGA pins have been allocated, and the board schematic design is nearing completion, it is very good practice to run the FPGA design through the vendor synthesis and placement tool suite before beginning the PCB layout.
Usually the FPGA RTL design is nowhere near completion; however, it’s good to generate at least a useable framework of the RTL design, which at minimum allocates the proper I/O resources. Developers typically make every effort to properly map each I/O peripheral to a specific bank and assign any clocking signals to the appropriate pins, but there are often device limitations that are only apparent if you’ve had the time to read all 300 pages of all ten user guides. Simply running this FPGA framework through the FPGA tool suite can help uncover these limitations with the DRC. Most of the limitations can be seen in lower-cost devices; for example, some pins are setup for inputs only, or in the specific case of the Xilinx Spartan-6 FPGA, only banks 0 and 2 can accommodate LVDS outputs, while every bank can handle LVDS inputs. Once the board goes to the layout stage, hardware engineering might decide that the routing will be much easier if DDR3 data pin 1 is swapped with data pin 15, for instance. It’s always good practice to run this change through the tool suite to see if it passes all checks.

**EECatalog:** We’ve talked about a lot of board design issues, but what about choosing the FPGA itself – are there specific factors developers should consider?

**Ferraro:** Often our customers are predisposed to one FPGA vendor or another, typically based on past experience or reputation. Whatever the case, there are many factors to analyze with respect to cost. Those include the number of I/O, size of logic resources, maximum internal clock rate, maximum general I/O clock rate, availability and quantity of SERDES pins, size of the package and configuration options. The analysis of the I/O peripheral and logic design that we perform up front, which we described previously, should help narrow the choice.

However, there are several other, less-obvious factors to consider before selecting the device. For instance, the data rates and clock rates quoted in the marketing material are often based on the highest speed grade available, and these devices often come at a premium. We review the datasheets to see the lowest speed grade the device is capable of. Another thing to look at is how I/O resources are grouped and mapped onto the FPGA pins. For example, a device might have 240 I/O that might be in three banks of 80 pins or six banks of 40 pins. If your design has multiple I/O standards – such as 1.5V for DDR3, 1.8V HSTL for Ethernet, 2.5V LVDS for ADC/DAC and 3.3V for CMOS – the number of banks will be important.

**Dietrich:** We typically make the FPGA vendor decision based on a few main factors. The technologies they offer are important, of course, but we also consider the support given by that vendor’s FAEs and online resources. Design software is another big component – each vendor will use a different set of tools, so you may want to use what you are most comfortable with or what has the best features for your needs. This is important because you’ll be spending a lot of time with these tools. And, of course, there’s cost and delivery. If you’re new to procuring FPGAs, you might be surprised to discover that vendors typically advertise new parts very early, and you may not actually be able to get your hands on one until a much, much later date.

And don’t forget to consider your upgrade path – this can often be overlooked in the early stages of the design but can turn out to be a real advantage if leveraged properly for your product. Some FPGA devices will have a pin-compatible upgrade path with other parts from a vendor’s series of FPGAs. This might mean that you can select a device for your original design that has fewer resources and is less expensive, but if needed, you can also populate a larger device in the future to accommodate larger FPGA designs. Or if the RTL design simply outgrows the selected part in terms of logic capacity, you want to make sure there’s a high-density part available in the same footprint.

**EECatalog:** Ultimately, what’s the key to a successful FPGA-based design?

**Ferraro:** When it comes to FPGA-based products, it’s often FPGA I/P, size, form factor and a few custom analog circuits that are the differentiating factor from one product to another. The FPGA’s I/O peripherals (memory, flash, Ethernet, etc.) might seem trivial because of their common and widespread use. But without careful consideration, their design-in could be the difference between a first-off functioning prototype (and happy customer) or the start of a lengthy re-spin process. Taking the right approach from the early stages – and asking all the right questions – will go a long way to ensuring a successful FPGA product design process.

Matt Ferraro is a senior hardware engineer and project manager at Connect Tech Inc., leading product development in embedded systems and FPGA computing solutions. He has a bachelor’s degree in computer engineering from the University of Waterloo (Canada).

Patrick Dietrich is a hardware design engineer and project manager at Connect Tech, Inc. Patrick has many years of experience as a lead designer and project manager on numerous FPGA, PCI Express and embedded COM carrier products developed by Connect Tech. Patrick received a bachelor’s of science degree in systems and computing engineering from the University of Guelph in Canada. He is an IEEE member, a Licensed Professional Engineer, and an active member of the PC/104 Consortium’s Technical Committee.
XPedite2300 Virtex-6 FPGA XMC Module
and FPGA Development Kit (FDK)

By Extreme Engineering Solutions, Inc.

XPedite2300 Virtex-6 XMC Module

The XPedite2300 is a high-performance reconfigurable conduction- or air-cooled XMC module based on the Xilinx® Virtex®-6 family of FPGAs. With an x8 PCI Express interface, external memory, and high-density I/O, the XPedite2300 is ideal for customizable, high-bandwidth, real-time, streaming data applications.

XPedite2300 Features

The XPedite2300 features include:

- Xilinx Virtex-6 LX240T, LX365T, SX315T, or SX475T FPGA
- Conduction- or air-cooled XMC module
- Two channels of DDR3 SDRAM, up to 1 GB (512 MB each)
- 180-pin, high-density daughter card header for I/O signals, 40-pin daughter card header for high-speed serial signals

In conjunction with the XPedite2300, X-ES provides the XPedite2300 FPGA Development Kit (FDK) based on the AXI4 interface protocol. The FDK includes IP blocks, example FPGA designs, and software to control and communicate with FPGAs. All of the IP blocks included in the FDK interface to the industry-standard AXI4 interconnect. The FDK utilizes standard Xilinx and third-party tools – Xilinx ISE Design Suite and EDK, Mentor Graphics® ModelSim®, Synopsys® Synplify®. With support for the AXI4 interface protocol and industry-standard tools, customers benefit from ease-of-use and true IP reuse without being locked into a proprietary FPGA development environment.

FPGA Product Plans

X-ES is in the process of developing Virtex-7 based boards. The first Virtex-7 based board will be a 3U VPX board with an FPGA Mezzanine Card (FMC) site, and an optional Freescale QorIQ P2020 processor. Future XMC modules will be designed with the Virtex-7 FPGA and an application-specific I/O subsystem rather than supporting configurable I/O with proprietary daughter cards.

FPGA Development Kit (FDK)

Extreme Engineering Solutions (X-ES) provides an FPGA Development Kit (FDK) to support the requirements of high-performance, real-time, embedded streaming data applications and to simplify the FPGA development process. The FDK is comprised of the Hardware Development Kit (HDK) and the Software Development Kit (SDK). The HDK includes the HDL code and files needed to build FPGA images, while the SDK includes drivers and utilities to set-up, control, communicate with FPGAs.

The initial hardware supported by the FDK is the XPedite2300 XMC module. As other X-ES FPGA modules are released, the support for them will be added to the FDK. In the X-ES FDK model, FPGAs and processors are interconnected via PCI Express links.

Hardware Development Kit (HDK)

- Based on AXI4 interface protocol, all provided logic blocks support AXI4 interconnects
- Utilizes standard Xilinx and third-party tools – ISE, EDK, Mentor ModelSim
- Logic blocks provided for all external hardware interfaces
  - PCIe (high speed data transfer to a host PC)
  - External memory controller (access to on-board Flash for non-volatile storage)
  - DDR3 controller (general purpose memory controller for on-board dynamic memory)
  - I²C (controls access to on-board EEPROM, Real-Time Clock (RTC), temperature sensors, and GPIO)
  - UART (provides serial port capability)
  - Daughter card I/O (support for multiple uses: DAC, ADC, etc.)
  - Additional masters and slaves (custom IP blocks can be added with AXI4 and PCIe access)
- MSI-x interrupt controller (supports inbound and outbound interrupts)
- Device ID block (provides a linked list of capabilities present in the FPGA that host software can parse through to determine at runtime the capabilities present in the FPGA)
- High performance DMA controller
- Partial FPGA reconfiguration is supported
- Complete example designs provided
- Complete documentation

The non-proprietary HDK is designed to simplify the process of FPGA development and provides a framework to easily integrate FPGA algorithms. Ease-of-use is facilitated through the support of the AXI4 interface protocol and use of the latest generation Xilinx ISE and EDK tools. Support for the AXI4 interface protocol makes logic blocks readily reusable, and the Xilinx EDK provides a GUI which enables logic blocks to be connected graphically by dragging and dropping them into a design.

All X-ES logic blocks interface to the AXI4 interconnect. Standardizing on the AXI4 interconnect enables logic blocks in the HDK, from Xilinx, and other third parties to be used without modification, unlike other FPGA development environments.
that require modifications to the HDL code in order to create a working FPGA design.

AXI4 includes three interconnect protocols that support both memory mapped and streaming type interfaces:

- AXI4: A traditional single-address burst interconnect supporting up to 256 data beats per burst, the width of which is system dependent.
- AXI4-Lite: A subset of the AXI4 protocol that only sends one data word per transaction.
- AXI4-Stream: A data-streaming interconnect that supports unidirectional, high-speed data transfers.

The HDK includes example FPGA designs and pre-built FPGA images (.bit files). The Xilinx EDK allows quick and easy reconfiguration of the example designs to incorporate customer logic. All HDK logic blocks are written in VHDL.

The Software Development Kit (SDK) includes drivers, libraries, and utilities to support the control of and communication with FPGAs in the system.

A driver framework is provided for software developers. The provided FPGA driver queries the FPGA to determine the capabilities that are instantiated in the FPGA. Based on the FPGA capabilities it discovers, the FPGA driver loads capabilities drivers. X-ES provides capability drivers for the following FPGA capabilities:

- I²C
- GPIO
- RS-232
- Flash
- Daughter card interfaces (ADC and DAC)

These drivers can be used as is or as a starting point for software developers to create their own application. Customers can add additional capability drivers.

All SDK software is written in ANSI C. Source code is provided for SDK software. The SDK is supported on Linux and VxWorks running on Intel and Freescale hosts.

FPGA Tools
The following tools are used for development with the X-ES FDK.

- Xilinx ISE Design Suite 13.2
- Xilinx Embedded Design Kit (EDK)
- Synopsys Synplify: Version E-2011.03
- Mentor ModelSIM

Software Development Kit (SDK)

- Drivers to communicate with FPGA devices
- Utility and APIs to re-flash and set-up FPGA
- APIs to discover capabilities loaded into FPGA
- Support for VxWorks and Linux on both Freescale (QorIQ) and Intel (Core i7) processors
In our roundtable discussion, Vin Ratford, senior vice president of worldwide marketing and business development for Xilinx, Inc., and Shakeel Peera, director of marketing for silicon/solutions at Lattice Semiconductor, provide in-depth commentary on the latest FPGA technologies and development trends.

EECatalog: What are some of the implications for developers as FPGAs move to 28nm technologies and beyond?

Vin Ratford, Xilinx: While there are a number of implications for developers as they move to 28nm FPGAs and beyond, I’d like to focus on four areas that are changing dramatically and are all interrelated.

The first area is integration. The 28nm process node and beyond offers a tremendous opportunity for FPGAs to deliver the capacities developers need to overcome the exorbitant cost of designing and manufacturing ASICs while reducing their bill of materials (BOM) through integration. For example, we recently began delivering a 6.8-billion-transistor programmable logic device using 2.5D Stacked Silicon Interconnect technology that allows us to provide integration that is more than double what customers are used to. With increasing integration, developers have a greater number of clock domains to manage, they need to perform smart partitioning of their design within the FPGA and work with incremental design flows; and they’ll want to use, or reuse, greater amounts of in-house and third-party IP.

The second implication is that developers need to understand the relationship of static and dynamic power as they use FPGAs to integrate more of their board on chip. They’ll want to understand the correct usage of optimized blocks within the FPGA, and system design approaches that allow for maximum performance with the lowest possible power consumption. The challenge for our industry is to deliver the maximum number of transistors per die, but with usable performance. This is why Xilinx is building its 28nm devices on a HKMG process with low power. We get a 50% to 70% power savings without sacrificing performance or capacity and can deliver devices that operate at 1V nominally, providing the headroom to offer products characterized at 0.9V that offer dramatically lower power.

The third implication is that higher integration means dealing with higher levels of throughput given the higher amounts of data going on and off chip. Care must be taken to address up-front signal integrity, jitter and board layout both for high-speed serial communications that will run up to 28.05Gbps as well as very wide, high-performance parallel interfaces.

The fourth implication is much higher on-chip processing. More than ever, customers need to become familiar with techniques for parallel processing to achieve the highest system-level performance. Developers not familiar with parallel design need to become familiar with the advantages of operating at a lower clock frequency and exploring performance versus latency, versus power tradeoffs. They should look to their vendor for experience as well as the optimized blocks and resources to enable them to achieve highly scalable, high-performance designs.

Shakeel Peera, Lattice Semiconductor: 28nm and beyond technologies will enable greater logic capacity, performance and integration for those customers interested in the largest and fastest devices, and will greatly reduce the cost for the largest devices. Networking applications needing 100G-400G worth of system bandwidth, and highly intensive signal processing applications like military, radar and medical imaging will benefit from reduced cost/bandwidth.

However, there will be challenges as well, especially for those designs that do not need the largest and fastest devices:

- 28 nm wafer costs will remain high relative to more mature technologies, but will be offset by smaller die sizes and slowly improving defect densities. The net result will be that for the most cost-sensitive applications that do not need the largest and fastest devices, and where large bandwidths are not needed, customers will have to wait some time before costs come down to the point where it is worthwhile to shift from legacy or mature process technologies.

- Smaller process geometries inevitably come with the need to operate from smaller supply voltages for reasons of reliability. Customers will need to adjust to 0.9V or 1V core supply voltages, and they will see a diminishing number of higher voltage I/O standards being supported. The
## Oscilloscopes

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Price</th>
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<tbody>
<tr>
<td><strong>Best Selling Scope</strong></td>
<td>25MHz 2-ch + trigger standalone USB scope with 8&quot; color TFT LCD</td>
<td>$279</td>
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<tr>
<td><strong>New! 25MHz Scope + Logic Analyzer</strong></td>
<td>Scope, logic and spectrum analyzer, function generator, and AWG all in one!</td>
<td>$999.95</td>
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<tr>
<td><strong>60/100/200MHz Scopes</strong></td>
<td>2-ch USB scopes with 10MSa/s storage. Slim design. Huge 8&quot; color TFT LCD.</td>
<td>$615.89</td>
</tr>
<tr>
<td><strong>100MHz Scope</strong></td>
<td>2 channel 1GS/s 100MHz scope with 1MS memory. Free carry case!</td>
<td>$399</td>
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<tr>
<td><strong>2-ch 50/100MHz Scopes</strong></td>
<td>2 ch + trigger 50/100/200MHz 8-bit USB scope adapters. Inc. probes &amp; case.</td>
<td>$628.57</td>
</tr>
<tr>
<td><strong>50/100MHz MSOs</strong></td>
<td>2 channel 16 logic scope and analyzer. 2000 wfn/s refresh rate. Free carry case!</td>
<td>$899</td>
</tr>
<tr>
<td><strong>60MHz 1/8 MOSO</strong></td>
<td>60MSa/s scope, 200MS/s logic analyzer, 100MS/s pattern generator + TDR. USB-powered.</td>
<td>$239</td>
</tr>
<tr>
<td><strong>Tiny 10MHz Scope</strong></td>
<td>Easy-to-use thumb-sized PC-based 75MHz 50MS/s 8-bit USB isolated Windows/Linux scope.</td>
<td>$199.95</td>
</tr>
<tr>
<td><strong>20MHz MSO</strong></td>
<td>Mixed signal 100MHz scope + spectrum &amp; logic analyzer. Also available with a signal generator.</td>
<td>$1,359</td>
</tr>
<tr>
<td><strong>4-ch 60/200MHz Scopes</strong></td>
<td>Fast 4-ch 2GS/s DSO 5.7&quot; TFT color LCD, bandwidth to 200MHz LXI compatible.</td>
<td>$945</td>
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## Oscilloscopes (con’t.)

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<th>Model</th>
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<tr>
<td><strong>200MHz 2/12 MSO</strong></td>
<td>200MHz 1GS/s 2 channel scope, 12 channel logic analyzer, 500MHz, FFT and 2MB buffer.</td>
<td>$1,789</td>
</tr>
<tr>
<td><strong>2-ch 250MHz Scopes</strong></td>
<td>High-performance USB scope with 32/128MS buffer 1GS/s + AWG advanced triggering.</td>
<td>$1,765</td>
</tr>
<tr>
<td><strong>4-ch 350MHz Scope</strong></td>
<td>Picoscope 6000 series - 4 channel 8-bit 390MHz = ultimate 3-channel USB scope design by Pico Technology.</td>
<td>$4,625</td>
</tr>
<tr>
<td><strong>2-ch 12GHz Scope</strong></td>
<td>World’s fastest 2-ch 12GHz sampling scope for analyzing high-speed electrical signals.</td>
<td>$11,575.28</td>
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## Analyzers

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<tr>
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<tr>
<td><strong>NEW! Spectrum Analyzer for Apple iOS</strong></td>
<td>The first 2.4GHz ISM band spectrum analyzer for the iPhone, iPod touch, and iPad.</td>
<td>$99.95</td>
</tr>
<tr>
<td><strong>4-ch Economy Logic Analyzer</strong></td>
<td>Full-featured, compact, easy to use PC based 4-channel logic analyzer and signal generator. ScanaLogic2</td>
<td>$99</td>
</tr>
<tr>
<td><strong>I2C Tester</strong></td>
<td>Versatile USB2.0 PC protocol exerciser &amp; analyzer. Sample/drive protocol traffic for checking/analysis.</td>
<td>$699</td>
</tr>
<tr>
<td><strong>SPI Tester including quadSPI</strong></td>
<td>Serial protocol host adapter - SPI/dual-SPI/quad-SPI. 32MB buffer, 100MHz signal, 8-bit DPI.</td>
<td>$1,289</td>
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## Controllers

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<th>Model</th>
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<tr>
<td><strong>WinCE Touch Controller</strong></td>
<td>WinCE-based 7” TFT LCD programmable (V/B/C++) touch-control PC w/ multiple interfaces.</td>
<td>$398.30</td>
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<tr>
<td><strong>WinXP Touch Controller</strong></td>
<td>XP Embedded touch panel. Touch-input 15 inch TFT LCD 14V-pard Windows PC.</td>
<td>$897.39</td>
</tr>
<tr>
<td><strong>Industrial PCs</strong></td>
<td>Rugged, compact, pre-loaded, embedded PCs for space-critical, harsh environment &amp; critical 24/7 operations.</td>
<td>Call for Quote</td>
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## Signal Generators

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<tr>
<th>Model</th>
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<tr>
<td><strong>Tiny 100MHz Signal Generator</strong></td>
<td>Thumb-sized digital pulse and clock gen. 100MHz 1.5V to 5.0V output. 75MHz single shot.</td>
<td>$199.95</td>
</tr>
<tr>
<td><strong>6-in-1 Signal Generator</strong></td>
<td>Six signal generators in one small, USB powered package for generating analog &amp; digital signals easily.</td>
<td>$227</td>
</tr>
<tr>
<td><strong>2/20MHz Function Generators</strong></td>
<td>2-20MHz with sweep opt. Simultaneous display of frequency &amp; amplitude.</td>
<td>$341</td>
</tr>
<tr>
<td><strong>Low-cost 6GHz RF Signal Generator</strong></td>
<td>Fast 4-ch 2GS/s DSO 5.7&quot; TFT color LCD, bandwidth to 200MHz LXI compatible.</td>
<td>$4,648.48</td>
</tr>
<tr>
<td><strong>3-6GHz RF Signal Generator</strong></td>
<td>High-precision, extremely low-noise, portable 3GHz RF gen. Rapid time switching.</td>
<td>$1,995</td>
</tr>
<tr>
<td><strong>2GHz RF Source</strong></td>
<td>High-crystal accuracy/stability, wide range, low phase noise/leakage, serial ctrl.</td>
<td>$499</td>
</tr>
<tr>
<td><strong>20GHz RF Source</strong></td>
<td>10MHz-20GHz+ low noise microwave signal gen. High dynamic range, fast switching times.</td>
<td>$5,400</td>
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## Miscellaneous

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<tbody>
<tr>
<td><strong>Digital USB Microscope</strong></td>
<td>Handheld digital microscope/magnifier and camera/video for high quality inspection.</td>
<td>$59.95</td>
</tr>
<tr>
<td><strong>Power Supplies</strong></td>
<td>Wide selection of benchtop power supplies from 30V/1A to 1200W LXI units.</td>
<td>Call for Quote</td>
</tr>
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</table>

**Saelig Company, Inc.** Since 1988, we have been searching the world for unique, terrific value, quality components and equipment, to make electronics design easier. We have a remarkable portfolio of test equipment and components to help you at any stage of your project. Visit [www.saelig.com](http://www.saelig.com) for more information.
ubiquitous 3.3 I/O will be most threatened, and customers will have to make difficult design choices to manage the number of power management components to ensure they keep their high-voltage I/O in existence.

- There is a concerted effort to reverse the trend found in previous generation process-node reductions, whereby static power caused by leakage current has been increasing exponentially. With advances in HK-MG dielectrics, it is now possible to see an exponential decrease in leakage current. However, HKMG remains more expensive than other High-K Silicon Oxide Nitrate technologies, and it is not clear that dynamic power (and therefore total power) will exponentially decrease compared to mature processes, even though it is clear there is some total power reduction.

- To really benefit from die shrinks, one will have to give up I/O, as I/Os do not shrink as much as pure digital logic. I/O-to-logic ratios will continue to drop, as has been the case with prior generation process-node shrinks.

Overall, the biggest short-term benefit will be for those designers looking to reduce cost or power in large logic or bandwidth-capacity FPGAs. There will be future trickle-down effect for lower-cost FPGAs, but this will be a mid- to long-term after 28nm reliability, costs and yield stabilize to a much greater extent than where they are now.

**EECatalog**: What trends are developing around IP cores, especially for specific vertical market applications?

**Ratford, Xilinx**: Key trends Xilinx is seeing and adopting are in the areas of development, IP protection, verification and deployment.

In IP development, we are seeing growing adoption of ESL technologies, whether this is something like MathWorks or C/C++, in addition to the traditional RTL development. Moving to higher levels of abstraction enables much faster verification at the system level as well as design exploration and portability.

For IP protection, the IEEE P1735 working group is very active. Our customers and ecosystem want to use and distribute IP with their choice of third-party simulation and synthesis tools. Today if they are using Xilinx encryption they are locked into our flow. P1735 will enable interoperable exchange of protected IP between tool vendors, establish support requirements for encryption and leverage certificate-based key management standards.

For IP verification, we are seeing as well as adopting OVM/UVM to improve design and verification efficiency, validate data probability and tool/verification IP interpretability. And then with deployment, Xilinx is a huge proponent of ‘plug-and-play.' We see a lot of focus on standardization, particularly with the AMBA AXI4 interfaces, which we support on all our IP along with an IP-XACT repository for storing customer, Xilinx and partner IP. The goal is to make IP easier to find and deploy.

**Peera, Lattice Semiconductor**: The single most visible trend has been growing customer expectations for complex subsystem IP rather than building-block IP. Until a few years ago, in markets like wired and wireless communications, it was customary to provide building-block IP or interface-IP like PCI-Express, Tri-speed Ethernet Mac, FIR and so on, while for the video market it used to be color space conversion, gamma correction and the like. Customers most often sourced building-block IP from multiple sources to stitch together their own subsystems.

Today, there is increased expectation from customers for the FPGA vendor to provide tested and proven standards-compliant, subsystem IP; for example, complete Ethernet Layer 2 switches with high-availability seamless redundancy, complete RRH multimode signal-path IP, complete high dynamic-range image signal-processing pipeline for video, and so on. There is also an increased reliance and expectation in the ability of the FPGA vendor to provide the subsystem IP while the customers concentrate on providing value-added differentiation through more efficient and innovative system design. This requires FPGA vendors’ vertical marketing teams to be extremely knowledgeable about the customers’ own markets and the needs of their customers. Value propositions in vertical-market IP now include not only building-block or interface functionality, but building blocks and interfaces interoperating together as functional, standards-compliant subsystems that are able to differentiate themselves in speed, cost and power advantages for the customer.

**EECatalog**: As Intel and ARM work to penetrate each other’s traditional markets, how will that play out in the future of dual-architecture SoCs?

**Ratford, Xilinx**: The sheer gravitational force that smartphones and tablet volumes are having on the processing requirements of low-power applications is phenomenal. As this pulls ARM architectures into more processing-intensive arenas, many of the smaller, niche performance...
architectures are moving onto the sidelines, resulting in what seems to be an ARM vs. Intel playing field. Going back to the earlier mention of AMBA AXI4 interfaces, we see a lot of adoption and a huge ecosystem behind the ARM architecture for SoCs. That was an important factor for Xilinx when we chose the ARM architecture to integrate with our programmable logic, as I presume it was for the other vendors with dual-architecture offerings.

**EECatalog:** What are some of the trade-offs embedded developers are making around power consumption and price point using FPGAs?

**Ratford, Xilinx:** FPGAs push the envelope with regards to process technology, offsetting much of the delta between fixed-function ASIC-oriented implementations at older nodes and programmable logic. Generally speaking, we are now typically 2 to 3 process nodes ahead of the alternative silicon solutions. This takes the natural cost/transistor benefits of Moore’s Law to the level where you can argue that the FPGA price-per-function is on par or cheaper than ASIC alternatives if you compare total cost of ownership. In terms of opportunity cost in a competitive marketplace, waiting for an ASSP solution may be tough if you’re trying to keep up with the latest standards and still meet production schedules.

Also, as FPGAs embed full 28nm SoC processing systems next to programmable logic in a single die, or use technologies like 2.5D Stacked Silicon Interconnect to leapfrog Moore’s law, we can integrate more system functions such as ADC blocks or even cutting-edge 28Gbps SERDES in ways that will further catapult the BOM cost reductions for system architects to take advantage of, as well as push total power consumption and system performance benefits to new levels.

**Peera, Lattice Semiconductor:** The tradeoffs are clear: the higher the bandwidth needed, the higher the cost and power consumption, and this relationship is exponential, not linear. Designers have to make a cost/bit and watt/bit calculation to understand the optimal FPGA choice. Also, as die sizes shrink, packaging costs will become an increasingly larger portion of the total chip costs, and these come down much more slowly than die costs. As such, suppliers will push to reduce overall BOM costs by pushing towards more aggressive packaging technologies that have copper wire bonds (shifting from gold), smaller ball pitches, less substrate layers and less on-package thermal enhancements.<0.8mm ball pitches, wafer level chip scale packages for small FPGAs and lidless flip chips are a recent phenomenon in the FPGA universe that highlight this trend, and PCB production techniques will have to keep up with this.

The single most visible trend has been growing customer expectations for complex subsystem IP rather than building-block IP.

Cheryl Berglund Coupé is Editor of EECatalog.com. Her articles have appeared in EE Times, Electronic Business, Microsoft Embedded Review and Windows Developer’s Journal and she has developed presentations for the Embedded Systems Conference and ICSPAT. She has held a variety of production, technical marketing and writing positions within technology companies and agencies in the Northwest.
Six Ways Synthesis Can Support Design Assurance in FPGAs

By Ehab Mohsen & Michelle Lange, Mentor Graphics

Use of FPGAs is on the rise, including in safety- and mission-critical applications, which previously were the exclusive realm of ASICs. As a result, FPGA designers are continually trying to improve their implementation methods to ensure safe circuit operation; work that’s spurred in part by enforcement by the regulatory authorities worldwide of safety standards such as DO-254 to ensure safety of in-flight complex hardware. These and similar standards in other countries (e.g., ED-80 in Europe) provide design assurance guidance for airborne electronic hardware; guidance that’s most commonly applied to PLD, FPGA and ASIC designs.

But aviation is just one example. Industry segments including military, automotive, space, medical, nuclear and transportation all have similar standards or concerns. The common objective of such standards is generally to ensure that the device produced will perform its intended function (as specified by requirements) under all foreseeable conditions. The development process itself becomes a big part of the proof. This means that FPGA designers and project leads are in effect frequently tasked with a twofold challenge—to not only meet a high standard of product reliability but also to prove that the proper planning, documentation, design and verification activities have been undertaken.

Selecting the right methodology and tool flow are among the most important decisions that must be made before initiating a DO-254 or other safety-critical project. No methodologies or tools are inherently certified, compliant or qualified for these types of programs. However, many companies that are concerned about design assurance are reevaluating their design methods and tools since both play an important role in overall program compliance while affecting productivity, schedule, budget and design quality.

Design Assurance—The Fourth Dimension of FPGA Synthesis

While requirements tracking and functional verification get much of the attention in design flows, the synthesis stage is of similar if not greater importance. After all, it is synthesis that takes the work of the designer and ultimately generates the corresponding hardware gates to be placed and routed in silicon. This entails not only ensuring functional equivalence of those gates to the original RTL created by the designer, but also the addition of safety features such as triple modular redundancy (TMR) when appropriate. Accordingly, before engaging in the actual design work of a safety-compliance project, it’s critical to understand how synthesis works and the broader context in which it is used.

Fortunately, when it comes to FPGA implementation, new synthesis automation technologies are helping to simplify and automate the compliance effort.

However, many engineers consider synthesis to be a “black-box” process that is difficult to understand or control. Optimizations take place under-the-hood, and designers almost never have time to become experts on synthesis algorithms. Fortunately, when it comes to FPGA implementation, new synthesis automation technologies are helping to simplify and automate the compliance effort.

Design projects typically have stringent implementation requirements, which historically have been placed into three categories: timing performance, design area and power. Tools that address each category generally serve the needs of most design flows. However, even seemingly full-featured synthesis tools may fall short in safety-critical domains, which require such stringent design assurance that it should be considered the fourth dimension of FPGA synthesis requirements. If this aspect of synthesis is not well-understood and managed, designers can compromise their ability to ensure the final implementation matches the design intent. This in turn means noncompliance with...
the basic objective of DO-254 and similar standards, which is to ensure the design performs its intended function.

The design assurance features pertinent to synthesis can be broken down into six main categories, as described in the following sections.

**Repeatable Synthesis Results**

DO-254 and similar standards require that each step in the process be repeatable. Repeatability fosters confidence, since rerunning these same steps in the same environment should yield the same design results every time. Historically, synthesis is one step in the design flow that has commonly yielded different results even when the same tool version and settings are used. It can be understandably alarming when each synthesis run creates different internal data structures and non-repeatable results. The way around such variability, and to produce a consistent netlist time after time, is to use a synthesis tool that relies on deterministic object name generation and is extensively tested for repeatability. To ensure the same compute environment (a prerequisite for repeatability), the tool should automatically generate documentation describing the hardware, operating system and tool settings to ensure repeatable netlist generation.

**Optimizations and Verifiable Synthesis Results**

In any design process, if a synthesis tool is trusted, then it is more or less assumed to produce a gate-level design that is functionally equivalent to the RTL written by designers and input to the tool. However, in a safety-critical process, there should be no “trust.” Instead, the output of every step and every tool should be reviewed or verified.

Synthesis performs various optimizations to reduce area and optimize performance in order to fit the design into the smallest and least expensive device. In most cases, these optimizations are beneficial; however, in high assurance design flows, they can make verification difficult. An optimization may improve area and performance but lead to simulation mismatches when comparing netlist to RTL test bench results.

Some synthesis flows now support a “design assurance mode,” which avoids tool settings and turns off optimizations that are not readily verifiable or may introduce simulation mismatches. Among the settings and optimizations important to turn off are the treatment of incomplete sensitivity lists, parallel/full case pragmas and four-state values (‘X’ or ‘U’ or ‘W’ or ‘Z’) for assignment or comparison.

**Logic Equivalence Checking**

While gate-level simulation is a generally accepted approach for large and complex designs, running the entire test bench with full timing can be incredibly time consuming. An alternative and much faster method of verifying synthesis results is using logical equivalency checking (LEC). LEC utilizes mathematical techniques to analyze one design model (in this case, the gate-level netlist generated by synthesis) against another (the thoroughly verified RTL code used as input to synthesis).
Using LEC on FPGA designs requires that the FPGA synthesis tool has an established working flow with a formal verification tool, mostly to share information about optimizations and methods for cross referencing these between the RTL and gate-level netlist. Such optimizations include merged, duplicated or inferred registers; re-encoded finite state machines; or inferred counters. Without this integration, setup for the LEC process can be tedious and subject to human error.

**Requirements Tracing**

DO-254 programs and the like use a requirements-driven engineering process. Requirements must be captured, validated, managed and traced to implementation and verification activities. Synthesis-related requirements, such as those that are performance-based, can be specified as constraints for the synthesis and place-and-route processes. For example, a set of synthesis constraints may implement a certain timing requirement, such as a dual-clock domain. Manually tracing these requirements down into the result files would be time consuming and could easily lack synchronization with current project results.

Some current tools can automate the process of tracing requirements to synthesis constraints, and through to the corresponding area and timing results from synthesis and place-and-route. An advanced synthesis tool can recognize requirement identifiers in the constraint definition files and insert references to these within the corresponding sections of the run reports, thereby generating automatically generated traceability reports.

**Mitigating Soft Errors (Including SEUs) with Triple Modular Redundancy**

Soft errors, such as single event upsets (SEUs), have become pervasive enough that companies complying with...
DO-254 are now encouraged to examine and address the issue of circuitry prone to radiation effects. Upcoming policies – see for example the imminent standards ARP 4754A and ARP 4761A, for development and safety analysis of aircraft systems, respectively – are evolving to more explicitly address the concern, generally by applying one or more mitigation techniques.

The latest synthesis technologies can automatically mitigate soft errors through implementation of triple modular redundancy (TMR) circuitry. TMR is a widely accepted method of fault-tolerant design in which a unit is triplicated and fed into one or more majority voter circuits. If an upset occurs on any one unit, the majority voter(s’) value will be the correct value and hence mask the fault.

Synthesis-based TMR can protect against both SEUs and single event transients (SETs are rogue voltage pulses that propagate through a combinational circuit) by triplicating some or all the design, depending on the design requirements. Synthesis is an ideal stage at which to make intelligent decisions about what to infer and when. For example, the synthesis tool can decide whether or not to infer embedded shift registers and how to treat synchronizers across different clock domains. Using a flow-based mitigation solution opens up device options to more SRAM, flash and antifuse devices from multiple device vendors, thus allowing project teams to more easily meet their capacity budget and performance requirements.

Reviewing Design Data and Tool Messages
Design reviews and audits occur throughout DO-254 and safety-critical processes. It becomes more difficult to review the actual design data in netlist format (post-synthesis), and yet this is when much valuable information about the design is finally known. As a synthesis tool transforms the design from RTL to gates, it finds useful information like constraints, clock domains, multi-cycle paths and how the RTL code was interpreted. Instead of reviewing the netlist itself, mining design data from the synthesis process can provide a wealth of useful information. As just one example: since design assurance requires that all the warnings reported by design tools be documented and explained, all the messages reported by the synthesis tool need to be properly categorized as warnings, errors or information messages.

Conclusion
Safety compliance is a challenge that’s not going away for an increasing number of aerospace hardware developers and those in many other industry segments. The ability to establish certifiable and highly productive design flows can be the difference between companies that are successful in this market and those that fall by the wayside. Design assurance is an essential element of these flows. The best bet, then, when getting started in design assurance? Pick a synthesis flow that goes beyond the usual design optimization goals and specifically focuses on those aspects of the design most important to safety-critical or design-assurance guidelines.

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Machine Vision – Making the Leap from Frame Grabbers to FPGAs

By Jake Janovetz, President, Opal Kelly

In the world of high-speed, processing-intensive machine vision, traditional frame grabbers are quickly losing ground to sleek, fast, ultra-capable FPGAs. Not so long ago, the best way to capture an image from a camera or image sensor for use in signal processing was to use an off-the-shelf frame grabber that sat inside a large desktop PC taking up a PCI slot. The expensive frame grabber would "talk to" an expensive CameraLink camera and deliver the image through some expensive software to the algorithm running on the PC. Thankfully, those days are over for the FPGA-savvy designer.

Traditional Machine-Based Inspection Systems
Consider the typical system, outlined below, composed of a machine under inspection. This machine could be inspecting a completed product, qualifying raw materials or simply measuring items for binning or sorting (such as mail or packages). In this example, the machine system also requires feedback from the image analysis to perform mechanical steps such as accept/reject or material routing.

The image system here, typically used in an assembly line, is based on a legacy frame grabber and requires a compatible camera, the frame grabber hardware, a desktop PC and some additional controller boards to feed decisions back to the machine. In a typical system of this sort, the image analysis is subject to at least one full-frame delay, and likely many more, due to the interfaces between the image sensor and the logic in the desktop PC that performs the analysis.

FPGA-Based Inspection Systems – Lower Cost, Lower Overhead
In contrast, consider the FPGA-based system below. Here the PC, frame grabber, camera interface logic and controller logic have all been replaced by a single, much lower-cost FPGA module. The desktop PC may remain as

![Diagram of Traditional Frame-Grabber Approach to Machine Vision](image-url)

Figure 1: Traditional Frame-Grabber Approach to Machine Vision
an optional device for remote monitoring or logging, but is generally not required. In a typical assembly line, many such FPGA-based cameras could all share the same PC hardware.

**FPGAs – Perfect for Image Capture**

Today’s image sensors come in all shapes, sizes, speeds and spectra. From low-cost CMOS visible-light image sensors, such as those in webcams, to line sensors for machine vision to upper-IR sensors that can “see” through human blood; the array of available image sensing technologies is nothing short of spectacular. The applications making use of them are even more prolific. Just as the image sensing market has grown exponentially, FPGA capability has come into its own with part densities quite capable of handling many image-processing tasks at speeds outpacing the dataflow produced by these sensors. FPGAs can talk directly to the image sensor, perform configuration tasks, manage vast memory spaces for capture and processing, filter, correct, compress, detect and so on. And since all this logic is in a single device, they do it with much less overhead than comparable multi-part, frame-grabber-based hardware. Fewer components between the image sensor and processing element also mean less dependence on third-party hardware, software and drivers.

**Machine Vision Capture Using FPGA**

Let’s first consider the capture side of the challenge in a typical machine-vision application. An image sensor is available that perfectly suits the requirements, but has a configuration interface (SPI and I²C are common) that needs to be utilized to realize the full functionality of the device. Setting up frame rates, calibration parameters and region of interest (ROI) are common functions performed over the configuration interface and can be crucial to realizing the optimal performance of the sensor. FPGAs handle this task natively and can even make use of tiny synthesizable sequential processors to make this easier. Frame grabbers need specific support for whichever interface is available, and that support may require vendor support for the chosen sensor.

Once the sensor is configured properly, the next task is image extraction. Grayscale sensors typically send out streams of pixel words. Color sensors do the same, but in a particular color sequence defined by the physical filtering installed. Again, the FPGA can handle this task directly and can very easily manage the various pixel-packing techniques employed. Since the FPGA is as close to the sensor as possible, it also has a dramatic latency advantage over a frame-grabber solution, which may have full frame (or more) latency to deal with. In certain machine-vision applications, latency can render a problem intractable or downright infeasible.

**The Processing and Analysis Landscape**

Once image data is streaming into the processor, applications split into a fractal landscape. Some applications simply need to relay the captured image to a PC for storage or processing. For these applications, the frame grabber is capable enough is but at least an order of magnitude more expensive in comparison to small, USB-attached FPGA modules. Other applications benefit from post-capture processing to handle filtering, detection or compression. Many frame grabbers also have FPGA capability and can be used for these tasks as well – again, typically at a much higher price than smaller FPGA integration modules.

With the proper development tools, FPGAs can perform ALL the typical tasks for image processing: demosaicing, color correction, white balance, matrix operations for sharpening, smoothing, etc., feature-detection, frequency-domain filtering and compression (JPEG, RLE). Even when tethered to a capable PC, these devices can off-load significant processing to the FPGA.

But where all-FPGA implementations really shine are tasks that involve feedback or control, such as machine management, part rejection and general quality control systems. Here, a tight closed-loop allows the system to run at high speeds and a compact, low-cost implementation allows the system to be replicated across an entire assembly line or multiple assembly lines.

An excellent example of closed-loop machine vision inspection is commonly performed in the wood industry to accept, reject or classify sawmill products prior to shipment. In this application, a small image-sensor board is
mated to a widely available, off-the-shelf FPGA module with USB interface.

The sensor captures images from a laser-scanned segment of wood as it passes the inspection camera. Capturing a small ROI at very high frame rates, it processes them to enhance sample classification capability using the Tracheid Effect.

Consisting only of a lens, image sensor board, FPGA module and enclosure, the complete camera is small enough so that four cameras may be installed on the same machine in tight quarters.

The resulting four-camera system is capable of continuously scanning wood samples as they pass through the machine, processing regions of interest at 2,400 frames per second. Not only is all of the image acquisition and processing logic contained within the FPGA, but leftover resources were available to control other aspects of the machinery, such as quadrature encoders and photocells; so that location information may be encoded directly with the image data sent to the PC.

Future Direction
Thanks to the low barrier to entry for FPGA design, the widespread availability of low-cost, value-add, off-the-shelf FPGA modules, and design IP and tools, the clear way forward for machine vision is away from expensive, bulky, low-capability frame grabbers and towards the supremely capable world of flexible hardware. In the past several years, I’ve personally witnessed a number of customers migrate their frame-grabber designs to FPGAs. There’s always an associated learning curve, but the benefits of tightly coupled integration and easy access to new, low-cost CMOS image sensors make the investment worthwhile.

I would like to thank Erik Vanserum for offering his permission to share these images in this article. For a detailed look at the construction of a machine vision system for this application, see Erik Vanserum’s article here: http://www.opalkelly.com/customers/vanserum/.

Jake Janovetz is founder and president of Opal Kelly Incorporated. Jake received his master’s degree in electrical engineering from the University of Illinois in 1999.
In the protocol world for communicating between integrated circuits, serial peripheral interface (SPI) has become a favorite, versatile choice for IC manufacturers because of its simplicity, especially when it comes to streaming large quantities of data with minimum pin count.

SPI is based on four signal lines (see Figure 1):
- One clock signal (SCLK) sent from the bus master to the slave(s); this clock is active when data is exchanged between master and slave
- One slave select (SS) line for each slave used to select the slave the master communicates with
- One data line from master to slave ('Master-Out-Slave-In' - MOSI)
- One data line from slave to master ('Master-In-Slave-Out' – MISO)

SPI is also a primary choice for electronics engineers when choosing a simple interface between ICs. As a de facto standard, however, the SPI protocol does not define much at all – no specific addressing scheme, no specific higher level formatting. Early on, the data length was 8 bits (1 byte), but now it can be almost any length.

There are many advantages to using SPI protocol:
- Clock rate is not restricted: within the IC’s physical limits, raising the clock rate increases the data rate.
- The protocol is full-duplex: data can be received as data is sent.
- It is equally suitable for many applications from register access with a fixed addressing/data scheme to the streaming of large amounts of data.
- SPI does not define the I/O voltage.
This protocol also presents some drawbacks: for advanced uses, it requires building full protocol stacks from scratch (SPI does not define anything) and it lacks a built-in acknowledgement mechanism.

Over time, SPI has seen variants and extensions – here are a few examples:

- The clock signal is sometimes generated as a continuously toggling signal, as the SS line can allow detecting when data is sent and not sent.
- Some variants merge MOSI and MISO data lines, implementing a half-duplex SPI protocol with a bidirectional data line (often referred to as ‘3-wire SPI’).

Dual-SPI and quad-SPI protocols are more or less standardized extensions of the SPI protocol. They are based on the following principles:

- Especially for flash memories, dual-SPI and quad-SPI protocols were created to increase the available bandwidth. Because they use multiple data lines in parallel, dual-SPI and quad-SPI protocols cannot strictly be considered as ‘serial’ protocols.

- Standard SPI protocol is used by default by dual-SPI and quad-SPI protocol slaves.
- Specific SPI instructions are used to set the slave in dual-SPI or quad-SPI mode.
Once the slave is configured in dual- or quad-SPI mode, the data transfers (read or write) use some additional control lines as data lines, resulting in a data bus extended from 1 data signal line to 2 (dual-SPI) or 4 (quad-SPI) data lines. Of course, the purpose is to increase the available bandwidth (see Figure 2).

**Non-Standard Serial Protocols**

Designing custom ICs such as ASICs, SoCs or FPGAs allows the choosing of standard or custom protocols for IC-to-IC communications. Typical differences between these protocols and standard SPI include:

- Higher levels of protocol stacks can be implemented in the communication protocol itself, requiring a more strict use of the clock and control lines.
- Specific data pulse sequences, with or without clock can be used to set the slave components into specific modes, or to ‘wake them up.’
- Open-drain I/Os are possible.
- Additional data lines can be used (e.g., quad-SPI).
- Other implementations reduce I/O pin-count and require bi-directional data lines.
- Edges used for data generation and sampling vary from what is specified for SPI.

**Development Tools for Protocols Beyond ‘Standard’ SPI**

There are a number of USB hardware solutions to provide standard SPI master and/or slave capabilities to computers running Linux, Mac or Windows, but hardly any of them work with quad-SPI. SPI host adapters create an SPI master on an SPI bus from almost any PC, and are great for embedded system, chip (FPGA/ASIC/SoC) and peripheral testing, programming and debug.

But, ideally, what is needed is a USB-connected serial protocol host adapter for PCs that supports not only standard SPI but also 3-wire SPI, dual-SPI and quad-SPI protocols as a master, allowing the control of custom serial protocol interfaces up to, say, 100MHz. This would allow access to ICs and embedded systems with standard and extended standard protocols, as well as user-defined methods, through graphical user interface PC software. It is extremely helpful to be able to view chip-to-chip communication protocols as an assembly of simple ‘segments’ characterized by ‘properties’ in terms of clocking, signal lines, control lines behavior, data sampling and data generation. Another useful feature would be a large memory buffer to allow some form of data logging and to guarantee accurate real-time signal generation and data sampling for most applications.
SPECIAL FEATURE

SPI host adapters are useful for troubleshooting digital designs, accessing registers and streaming serial port data; exercising ICs and embedded systems that use serial protocols; programming SPI, dual-SPI and quad-SPI flash memories; accessing ADC, DAC and other components that use standard SPI protocols; and accessing custom chips (FPGA, ASIC) using non-standard protocols for IP testing and prototype validations. Some available adapters provide useful GUI applications to make SPI access user-friendly. APIs also often are provided for use with other software. An included GPO/pattern generator with a dedicated memory can provide helpful input digital vector generation.

Many high-end scope manufacturers offer scope-based triggering and protocol decode for SPI protocols, and most support 2-, 3- and 4-wire SPI, but these are often optional (i.e., not free) extras. PC oscilloscope adapters and logic analyzers also often offer SPI decode capabilities, but do not provide master capabilities.

Non-Standard Protocol Definition

It is helpful to be able to create a non-standard SPI protocol to match a new capability or a manufacturer’s unusual communication standard, but creating or reproducing this can often be challenging. The Studio software, provided with the SPI Storm allows a visual creation and definition of protocol parameters.

Protocol Defining Software

Once the protocols are defined in the GUI software, the user can choose to setup and execute

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>SPI Host Adapter</th>
<th>Host Bus</th>
<th>Bus List</th>
<th>Max frequency</th>
<th>Price USD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte Paradigm</td>
<td>SPI Storm</td>
<td>USB</td>
<td>SPI, SPI 3 wires, dual-SPI, quad-SPI, custom protocol, GPO</td>
<td>100 MHz</td>
<td>$1,199</td>
</tr>
<tr>
<td>Byte Paradigm</td>
<td>SPI Xpress</td>
<td>USB</td>
<td>SPI, SPI 3 wires</td>
<td>50 MHz</td>
<td>$699</td>
</tr>
<tr>
<td>Diolan</td>
<td>U2C-12</td>
<td>USB</td>
<td>I²C, SPI, GPIO</td>
<td>200 kHz</td>
<td>$89</td>
</tr>
<tr>
<td>National Instruments</td>
<td>USB-8541</td>
<td>USB</td>
<td>I²C, SPI</td>
<td>12 MHz</td>
<td>$109</td>
</tr>
<tr>
<td>Total Phase</td>
<td>Aardvark</td>
<td>USB</td>
<td>I²C, SPI</td>
<td>8 MHz</td>
<td>$250</td>
</tr>
<tr>
<td>Total Phase</td>
<td>Cheetah</td>
<td>USB</td>
<td>SPI</td>
<td>40 MHz</td>
<td>$350</td>
</tr>
</tbody>
</table>

Table 1 SPI Host Adapters

Figure 6: Defining custom protocols in "SPI Storm Studio" software

Figure 6: Defining custom protocols in "SPI Storm Studio" software
real access sequences with the graphical user interface or with C-function calls from the provided API.

This enables task automation and building complete custom application interfaces from an environment that can call standard C functions.

Conclusion
Standard and custom serial protocols used for chip-to-chip communications are ubiquitous. Finding a convenient and powerful tool that enables ASIC, SoC and full embedded system development, testing and debugging can be an additional challenge, however. It is often necessary to be able to define unique serial protocols or fine tune the characteristics of standard protocols such as SPI. It is often helpful to try a demo version of the manufacturer’s software before you buy it.

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Alan Lowne is CEO of Saelig Co. Inc. (Pittsford, NY), a North American distributor founded in 1988, which sources and supports unique control and instrumentation products from around the world. Prior to forming Saelig, Alan worked as an analog/digital design engineer for Eastman Kodak Co. in UK and USA, working on digital photography and clinical instruments. He completed electronic engineering degrees from Southampton University (UK) and Brunel University (UK).
FPGA Verification Must Address User Uncertainty for Prototyping, System Validation

By Loring Wirbel, Footwasher Media

The recent expansion and diversification of the FPGA verification market bears a certain resemblance to the ASIC verification market of 20 years ago, though beset with opposite challenges, thanks to the changes wrought in 20 years by Moore’s Law. When companies such as Quickturn Systems created large logic emulation systems to verify ASICs in the early 1990s, users had to be convinced to spend significant amounts of money while dedicating floor space equivalent to a mainframe, all to verify system ASICs. Today, FPGA verification can be addressed in add-in boards for a workstation, or even in embedded test points within the FPGA itself (see http://www.element14.com/community/docs/DOC-37820/l/tektronix-moves-to-integrate-single-chip-functionality-through-instrumentation).

But even as customers in 1990 were reticent to move to logic emulation due to price tags, today’s FPGA verification customer may show some trepidation because such systems may seem simplistic, invisible, or of questionable value (see http://www.element14.com/community/docs/DOC-37823/l/commentary-misconceived-missed-opportunities-in-fpgas). In many cases, however, FPGA users dare not commit to multiple-FPGA systems (see http://www.element14.com/community/docs/DOC-37937) – or to ASICs prototyped with FPGAs – without these tools. Newer generations of FPGAs incorporating the equivalent of millions of gates, integrate RISC CPUs, DSP blocks, look-aside coprocessors, and high-speed on-chip interconnects. Verification of such designs is a necessity, not a luxury.

On the software-only front, all major FPGA vendors, as well as three of the major EDA suite vendors, offer “design for verification” tools that tie behavioral simulation to system-level test and test-regression analysis. While such tools are useful, at some point they must be combined with dedicated hardware that can tie specific FPGAs to system-level requirements.

The notion of an add-on card is the easiest conceptual hurdle for many designers to address. This can take the form of anything from a module that integrates an FPGA to that of a solid-state drive. However, the FPGA design community still must adopt a better feeling as to how FPGAs can aid in their own verification if they hope to have effective innovation available soon (see http://live-page.apple.com).

Products for characterizing SoCs are combined with synthesis language and IP libraries to give the designer an easy-to-configure platform for testing hardware ideas. What began as a means of prototyping other silicon devices has become a way to validate the FPGA itself; an indication of how the FPGA verification market can be used in bootstrapping a next-generation FPGA based on known designs.

Embedded instrumentation potentially can take designers to the next step by embedded hardware test points within their FPGAs or ASICs. The idea has been used in the past for testing chip designs through I/O pads; a concept that gave rise to the military JTAG standard. This idea is extended to FPGAs by using test points for verifying not only individual FPGAs, but the behavior of systems employing multiple FPGAs.

Since the newest generations of FPGAs incorporate millions of equivalent gates, embedded instrumentation may soon be necessary. At a minimum, however, FPGAs offering multiple asymmetric cores processing complex data sets in real time will require multiple complementary software and hardware verification tools to insure first-pass design success.

Loring Wirbel is a technology analyst with more than 20 years’ experience covering semiconductors, communications, embedded software, and any other topics that catch his fancy. In addition to his freelance work he contributes to several political and cultural journals and web sites.
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  Assorted tutorials, VHDL code and complete projects designed to assist students in the Johns Hopkins VHDL/FPGA class.

- [http://www.ece.cmu.edu/~ece545/F10/fpga_resources.html](http://www.ece.cmu.edu/~ece545/F10/fpga_resources.html)
  FPGA-related sites that feature granular information and guides on different mechanisms for programming FPGAs.

  FPGA hints, tips and tricks.

- [http://www.mrc.uidaho.edu/fpga/](http://www.mrc.uidaho.edu/fpga/)
  An extensive, searchable database on information pertaining to FPGAs.

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**Events**

**FPGA Summit / DesignCon2012**
Conference – Jan. 30-Feb. 2
Exhibition: Jan. 31-Feb. 1
[http://www.designcon.com/fpga_summit](http://www.designcon.com/fpga_summit)

**Embedded World Conference**
February 28 to March 1, 2012 - Nürnberg, Germany

**DATE 2012**
March 12-16, 2012 - Dresden, Germany

**ESC Conference**
March 26-29, 2012 - San Jose, CA
[http://www.ubmdesign.com/esc/conference](http://www.ubmdesign.com/esc/conference)

**FCCM 2012: The 20th Annual IEEE International Symposium on Field-Programmable Custom Computing Machines**
April 29 - May 1, 2012 - Toronto, Canada
[http://fccm.org/2012/](http://fccm.org/2012/)

**19th Reconfigurable Architectures Workshop**
May 21-22, 2012 - Shanghai, China
[http://www.ece.lsu.edu/vaidy/raw/](http://www.ece.lsu.edu/vaidy/raw/)

**DAC 2012**
June 3-7, 2012 - San Francisco, CA

**Flash Memory Summit 2012**
August 21-23 - Santa Clara, CA
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FEATURES & BENEFITS

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◆ A new standard for best cost for higher speed interfaces, including memories and transceivers
◆ Further cost reduction with the smallest footprint packages, leveraging wire bond chip-scale BGA technology.

TECHNICAL SPECS

◆ 1,040 DSP Slices enabling 1248 GMACs of performance
◆ Up to 16 High Speed serial transceivers supporting line rates up to 6.6 Gbps
◆ 3.3V capable I/O to enable interfacing to legacy components
◆ Low Cost wire-bound packaging
◆ Chip-scale packages for smallest form factor

AVAILABILITY

Visit www.xilinx.com/artix7 to learn more

APPLICATION AREAS

Automotive, Consumer, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications
Kintex-7 FPGA

Supported FPGA/CPLDs: 28nm based-product

Kintex™-7 FPGAs offer high-density logic, high-performance connectivity, memory, and DSP, plus Agile Mixed Signal all to enable higher system-level performance and integration.

Fabricated on a 28nm process, all 7 series FPGAs share a unified architecture. This innovation enables design migration across the Artix™-7, Kintex-7, and Virtex®-7 FPGA families. System manufacturers can easily scale successful designs to address adjacent markets requiring reduced cost and power or increased performance and capability. The adoption of AMBA 4, AXI4 specification as part of the interconnect strategy supporting Plug-and-Play FPGA design further improves productivity with IP reuse, portability, and predictability.

The Kintex-7 FPGA KC705 Evaluation Kit accelerates development and demonstration of radio/baseband, radar, EdgeQAM, triple-rate SDI and other applications for a broad range of markets that demand power-efficient high-speed communications and processing. Features include on-board PCI Express, Agile Mixed Signal (AMS), HDMI video output, and FPGA mezzanine card (FMC) connectors for smooth migration to the 7 series.

The Kintex-7 FPGA DSP Kit lets developers rapidly migrate to the 7 series using a platform that fosters innovative and highly differentiated solutions. Designers can reduce schedule risk, shorten time to market, and more quickly focus on adding unique value to solutions targeted for wireless communications infrastructure (remote radio heads, software-defined radio, DPG feedback, and more), aerospace and defense, instrumentation, medical imaging, and general-purpose data acquisition.

FEATURES & BENEFITS

◆ 28nm high-K metal gate (HKMG) process technology and a High-Performance, Low-Power (HPL) approach that drives up power efficiency
◆ Performance boosting innovations, including industry-leading 1,866 Mbps memory interface; 639 MHz DSP48E1 slices with high-performance filtering capabilities, combined with the six-input look-up table for flexible DSP designs

KINTEX<sup>7</sup>

◆ Dedicated hard memory Phy implementation provides a simplified interfacing to external DDR memory
◆ Package optimized to line rate performance
◆ A flexible, soft controller enabled by high-performance logic for calibration, access methods, and system interfaces

TECHNICAL SPECS

◆ 1833Mbps memory interfaces
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◆ Up to 1,920 DSP slices
◆ High-speed PCI Express hard and soft IP
◆ Integrated hard IP for PCI Express, with full support for PCI Express endpoint and root port configurations
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AVAILABILITY

To learn more about Xilinx Kintex-7 FPGAs please visit www.xilinx.com/kintex7

APPLICATION AREAS

Aerospace/Defense, Consumer, Medical Imaging, Wireless Communications

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Kintex-7 FPGA KC705 Evaluation Kit

Supported FPGA/CPLDs: Kintex-7 FPGA

The Xilinx Kintex™-7 FPGA KC705 Evaluation Kit accelerates development and demonstration of radio/baseband, radar, EdgeQAM, triple-rate SDI, medical imaging and other applications for a broad range of markets that demand power-efficient high-speed communications and processing. In order to help get you to market quicker Xilinx has designed in the ideal feature set including on-board PCI Express, Agile Mixed Signal (AMS), HDMI video output, and FPGA mezzanine card (FMC) connectors for smooth migration to the 7 series.

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FEATURES & BENEFITS

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◆ Integrated evaluation kit boosts developer, productivity with a combination of silicon, software, IP and reference designs
◆ Unified Architecture provides scalability and migration for maximum design reuse and immediate start on Kintex-7 as well as Artix™-7 FPGA designs

TECHNICAL SPECS

◆ KC705 Base Board with a XC7K325T-FF900-2 FPGA
◆ Full Seat ISE® Design Suite Logic Edition
◆ Reference designs and demonstrations (please see Xilinx.com for latest designs)
◆ Board Design Files and Documentation including a step-by-step Getting Started Guide
◆ USB Cables, Ethernet Cable, universal power supply, and AMS Evaluation Card

AVAILABILITY

To learn more about the Xilinx Kintex-7 KC705 FPGA Evaluation Kit and all Targeted Design Platform solutions, please visit www.xilinx.com/kc705

APPLICATION AREAS

Aerospace/Defense, Medical Imaging, Wireless Communications

CONTACT INFORMATION

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www.xilinx.com/artix7
Xilinx Agile Mixed Signal

 Supported FPGA/CPLDs: Xilinx 7 series FPGAs

The Xilinx 7 series Agile Mixed Signal (AMS) approach now delivers the industry’s most flexible general purpose analog interface. The programmable Xilinx Analog-to-Digital Converter (XADC) and logic enables customization for a wide variety of applications, from simple control and sequencing to more signal processing intensive tasks like linearization, calibration, and filtering. The signal processing capabilities of the FPGA can also be leveraged to enhance the performance of the Analog-to-Digital Converters (ADCs) using techniques like oversampling.

The Agile Mixed Signal is available in all Xilinx 28nm FPGAs, delivering application solutions for cost-sensitive and low power markets serviced by Artix™-7 FPGAs and Zynq™-7000 Extensible Processing Platforms as well as enhanced reliability in high performance markets served by Kintex™-7 and Virtex®-7 FPGA families.

The XADC is an independent, 1MSPS, 12-bit, analog-to-digital converter. In addition to general purpose analog integration, the XADC block also contains temperature and supply sensors that greatly enhance reliability, security, and safety capabilities of FPGAs.

The analog features are ideally suited for high-volume applications like multifunction printers, digital SLR cameras, motor control, power conversion, touch/gesture based HMI, anti-tamper security and system management and best serve the industrial, automotive, consumer, wireless, wired AVB, medical and aerospace and defense markets.

FEATURES & BENEFITS

- ADCs carry out 16-bit conversion with digital calibration
- Dual Independent Track & Hold (T/H) Amplifiers
- External or On-chip Voltage Reference
- On-Chip Thermal and Supply Sensors
- Precise user control of sampling instant & simultaneous sampling
- Supports UniPolar, Bi-Polar and true differential sampling
- Up to 16 analog inputs supported using dual purpose digital IO

TECHNICAL SPECS

- Dual 12-bit 1Msps Analog-to-Digital Converters
- ADC specified over full industrial temp range -40°C to +100°C
- DNL ±0.9 LSBs, INL ±2 LSBs, Gain Error ±0.4%, Offset ±4 LSBs
- On-chip voltage ref = ±1% error
- Temperature sensors with ±4°C max error
- Power supply monitoring with ±1% max error

AVAILABILITY

To learn more about Xilinx 7 series Agile Mixed Signal, please visit www.xilinx.com/AMS

APPLICATION AREAS

Aerospace/Defense, Automotive, Consumer, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications, AVB
Xilinx Transceiver Characterization Kits

Supported FPGA/CPLDs: Virtex-6 HXT, Virtex-6 LXT, Spartan-6 LXT

Xilinx® Virtex®-6 FPGA ML623, Virtex®-6 ML628, and Spartan®-6 SP623 Transceiver Characterization Kits simplify the evaluation of Xilinx GTH, GTX and GTP low-power, high-speed serial transceivers with the latest generation devices and Xilinx Targeted Design Platforms.

The kits provide hardware and software developers with everything needed to create and fully characterize designs with Virtex-6 FPGA GTH and GTX, and Spartan-6 FPGA GTP multi-gigabit transceivers, including the ML628, ML623, and SP623 characterization boards, ChipScope™ Pro IBERT reference design, PCB design files, and documentation.

The ML628 characterization board features access to 24 GTH transceivers with a high performance Virtex-6 HX380T FPGA. Virtex-6 GTH is ideal for highest bandwidth, low power applications with per-transceiver line rates from 1.24Gb/s to 11.18Gb/s. The ML623 characterization board features 24 GTX transceivers with Virtex-6 LX240T FPGAs. Virtex-6 FPGA GTX transceivers are ideal for higher bandwidth, low-power connectivity applications with line rates from 750Mb/s to 6.5Gb/s. The SP623 characterization board provides access to 8 GTP transceivers with low-cost, low-power Spartan-6 LX150T FPGAs that offer the lowest risk, lowest cost serial connectivity with line rates from 614Mb/s to 3.125G/ps. GTH transceivers are accessible through low-loss bullseye connectors; GTX and GTP transceivers are accessible via four SMA connectors per transceiver.

FEATURES & BENEFITS

◆ GTH and GTX transceivers offer the industry’s best signal integrity with eight programmable levels of Transmit Pre-emphasis and four programmable levels of Receive Equalization

◆ GTX transceivers are power-optimized for 150-180mW per transceiver with programmable Transmit Pre-emphasis and Receive Equalization

◆ GTH, GTX, and GTP transceivers are automatically configured with the Xilinx CORE Generator™ software to support different protocols or perform custom configuration

TECHNICAL SPECS

◆ ML628 characterization board with Virtex-6 HX380T-FFG1923 device

◆ ML623 characterization board with Virtex-6 LX240T-FF1156 devices

◆ SP623 characterization boards available with Spartan-6 LX150T-FFG676 devices

◆ Configured with SystemACE 2G CF card, JTAG, USB to UART bridge and USB host controller, LED displays, and control buttons/switches

◆ Industry-standard low-pin count FMC connector Selectable 1.0V or 1.2V VCCINT jumper cable and *3.3V, 2.5V, 1.8V, and 1.2V power supplies

AVAILABILITY

Available today at www.xilinx.com/kits

APPLICATION AREAS

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications
Xilinx Virtex-7 FPGAs

Supported FPGA/CPLDs: 28nm based-product

Virtex®-7 FPGAs are optimized for advanced systems requiring the highest performance and highest bandwidth connectivity. The Virtex-7 family is one of three product families built on a common 28nm architecture designed for maximum power efficiency and delivers 2X higher system performance at 50% lower power than previous generation FPGAs.

The Virtex-7 2000T FPGA delivers greater than 2X the capacity and bandwidth offered by the largest monolithic devices while delivering the time-to-volume advantages of smaller die. Utilizing innovative 2.5D Stacked Silicon Interconnect (SSI) technology, the Virtex-7 2000T FPGA integrates 2 million logic cells, 6.8 billion transistors and 12.5Gb/s serial transceivers on a single device making it the world’s highest capacity FPGA offering unprecedented system integration in addition to ASIC prototyping and ASIC replacement capabilities.

The Xilinx Virtex-7 FPGA VC707 Evaluation Kit gives designers an easy starting point for evaluating and leveraging devices that deliver breakthrough performance, capacity, and power efficiency. Out of the box, this platform speeds time to market for the full-range of Virtex-7 applications including advanced systems for wired and wireless communications, aerospace and defense, medical, and broadcasting.

FEATURES & BENEFITS

- Virtex-7 T devices deliver unprecedented levels of capacity and performance enabling ASIC prototyping, emulation and replacement
- Virtex-7 XT devices offer the highest processing bandwidth with high performance transceivers, DSP and BRAM
- Virtex-7 HT devices with integrated 28Gbps serial transceivers offer an unprecedented 2.8Tb/s of serial bandwidth
- Up to 2M logic cell capacity for building massively parallel high-performance circuits enabled by stacked-silicon interconnect (SSI) technology
- Reduced power enabled by new 28nm High-Performance, Low-Power (HPL) process, architectural enhancements, and advanced software

TECHNICAL SPECS

- Up to 2M logic cells, 6.8 billion transistors and 12.5Gb/s serial transceivers on a single device
- Up to 96 transceivers operating at 13.1Gbps, and 16 transceivers operating at 28.05Gbps raise I/O bandwidth to 2.8Tbps
- Up to 3,600 DSP48E1 slices raise DSP performance to 5.3TMACS
- Up to 16 x 28 Gb/s serial transceivers for ultra-high bandwidth applications
- Optimized for next-generation 100G, nx100G and 400G line cards with CFP2 optical interfaces

AVAILABILITY

To learn more about Xilinx Virtex-7 FPGAs please visit www.xilinx.com/virtex7

APPLICATION AREAS

Aerospace/Defense, Consumer, Data Processing and Storage, Wired Communications, Networking, financial, life science
Zynq-7000 Extensible Processing Platform

The Zynq™-7000 family is the world’s first Extensible Processing Platform (EPP). This innovative class of product combines an industry-standard ARM® dual-core Cortex™-A9 MPCore™ processing system with Xilinx 28nm unified programmable logic architecture. This processor-centric architecture delivers a complete embedded processing platform that offers developers ASIC levels of performance and power consumption, the flexibility of an FPGA and the ease of programmability of a microprocessor.

The four devices of the Zynq-7000 EPP family allow designers to target cost sensitive as well as high-performance applications from a single platform using industry-standard tools. The tight integration of the processing system with programmable logic allows designers to build accelerators and peripherals to speed key functions by up to 10x. ARM architecture and ecosystem maximizes productivity and eases development for software and hardware developers.

Unlike ASICs and ASSPs, Zynq-7000 devices allow designers to modify their design throughout the development phase and after the system is in production. In addition, the Zynq-7000 EPP family, with over 3000 interconnections between its processing system and the programmable logic, offers levels of performance that two-chip solutions (ASSP+FPGA) cannot match due to limited IO bandwidth and limited power budgets.

FEATURES & BENEFITS

◆ Dual ARM Cortex-A9 MPCore
  • Up to 800MHz
  • Enhanced with NEON Extension and Single & Double Precision Floating point unit
  • 32kB Instruction & 32kB Data L1 Cache
◆ Unified 512kB L2 Cache 256kB on-chip Memory
◆ DDR3, DDR2 and LPDDR2 Dynamic Memory Controller
◆ 2x QSPI, NAND Flash and NOR Flash Memory Controller
◆ 2x USB2.0 (OTG), 2x GbE, 2x CAN2.0B, 2x SD/SDIO, 2x UART, 2x SPI, 2x I2C, 4x 32b GPIO
◆ AES & SHA 256b encryption engine for secure boot and secure configuration
◆ Dual 12bit 1Mmps Analog-to-Digital converter
  • Up to 17 Differential Inputs
◆ Advanced Low Power 28nm Programmable Logic:
  • 28k to 350k Logic Cells (approximately 430k to 5.2M of equivalent ASIC Gates)
  • 240KB to 2180KB of Extensible Block RAM
  • 80 to 900 18x25 DSP Slices (58 to 1080 GMACS peak DSP performance)
◆ PCI Express® Gen2x8 (in largest devices)
◆ 154 to 404 User IOs (Multiplexed + SelectIO™)
◆ 4 to 16 12.5Gbps Transceivers (in largest devices)

APPLICATION AREAS

Automotive, Broadcast, Medical Imaging, Industrial Motor Control

CONTACT INFORMATION

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Spartan-6 FPGA Market Specific Kits

Supported FPGA/CPLDs: Spartan-6 LXT

Spartan®-6 FPGA market-specific kits provide all the elements needed to design right out of the box, enabling system designers to accelerate time-to-market and improve differentiation of lower power ‘greener’ products.

Spartan-6 FPGAs offer an optimal balance of cost, power, and performance for systems in consumer digital displays and broadcast connectivity.

Available Spartan-6 FPGA market-specific kits:
- Spartan-6 FPGA Consumer Video Kit 2.0
  - Optimized to efficiently develop and test high-speed serial interfaces and debug HDMI or DVI-based solutions. Enables rapid design to HD and 3D video standards such as HDMI 1.4a and V-by-One®HS.
- Spartan-6 FPGA Broadcast Connectivity Kit
  - Simplifies development of high performance broadcast audio and video interface solutions such as SD, HD, and 3G-SDI.

FEATURES & BENEFITS
- Comprehensive video algorithm development platform with all the hardware, software, firmware building blocks, and tools need to begin development right out of the box
- Targeted reference designs to kick-start design time for specific applications
- RoHS-compliant base board designed for high-bandwidth designs (8 SERDES channels)

TECHNICAL SPECS
- Spartan-6 LX150T Base Board
- FMC daughter cards (Consumer Video Kit): HDMI 1.4a Tx/Rx, DisplayPort, V-by-One® HS and LVDS
- FMC daughter cards (Broadcast Connectivity Kit): 4 channel Triple-rate SDI and 2 channel AES-3 Audio Tx/Rx
- ISE® Design Suite - Device Locked
- Documentation, set-up guides, reference designs, board diagnostics, cables, and power supply

AVAILABILITY
For the latest information on Spartan-6 FPGA market-specific kits as they become available, visit: www.xilinx.com/kits

APPLICATION AREAS
Broadcast, Consumer

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Virtex-6 FPGA Market Specific Kits

Supported FPGA/CPLDs: Virtex-6 HXT

Virtex®-6 FPGA market-specific kits provide all the elements needed to design right out of the box, enabling system designers to accelerate time-to-market and extend time-in-market.

Virtex-6 FPGAs provide the right mix of programmability, integrated blocks for DSP, memory, and connectivity support – including high-speed transceiver capabilities—to satisfy the insatiable demand for higher bandwidth and higher performance.

Available Virtex-6 FPGA market-specific kits:
- Virtex-6 HXT FPGA ML630 Evaluation Kit for OTN – Cost-effective development platform for 100G applications such as transponder, muxponder and ODU switching with a smooth migration path to 400G.
- Virtex-6 HXT FPGA ML631 Evaluation Kit for PP/TM – Cost-effective development platform for 100G applications in packet processing and traffic management applications.

FEATURES & BENEFITS
- Comprehensive development platforms with all the hardware, software, firmware building blocks, and tools need to begin development right out of the box
- Proven reference designs and trial-use access license for IP
- Superior transceiver performance with industry’s first optically-compliant programmable devices
- Smooth migration path to 7 series FPGAs

TECHNICAL SPECS
- Optically compliant Virtex-6 HXT ML630 and ML631 base boards
- HiTech Global CFP carrier cards and loopback module
- ISE® Design Suite - Device Locked
- Documentation, set-up guides, and reference designs
- Cables, power supply, and compact flash card

AVAILABILITY
For the latest information on Virtex-6 FPGA market-specific kits as they become available, visit: www.xilinx.com/kits

APPLICATION AREAS
Data Processing and Storage, Wired Communications
Tag-Connect Plug-of-Nails™
In-Circuit Programming
and JTAG Cables

Supported Architectures: PIC, dsPIC, MSP430, ARM, JTAG,
Atmel, Altera, Xilinx, FPGA’s and CPLD’s

Tag-Connect’s Plug-of-Nails™ cables provide a simple, reliable means of connecting Debuggers, Programmers and Test Equipment to your PCB’s while lowering board costs, reducing board space and facilitating efficient production programming.

Tag-Connect uses specially designed connectors which eliminate the need for a programming header or other mating connector on every PCB. Instead, Tag-Connect uses tried and tested spring-pins to make a secure connection to a special footprint of pads and locating holes in your PCB.

The PCB footprint can take up as little board space as 0.02 square inches (about the space needed for a couple of 0805 SMT resistors).

TC2030 6-pin and TC2050 10-pin series cables are available in both “Legged” and “No-Legs” versions. The Legged versions have feet that snap into your PCB for prolonged debugging or programming operations whereas the No-Legs versions are designed for fast and efficient hand-held operations and are well suited to production programming. A 20-pin cable is due in Q2 2011.

A growing range of adapter boards and cables makes these cables compatible with most families of MCUs, FPGAs and other JTAG devices including PIC, dsPIC, MSP430, ARM, ATMEAL, Freescale, Altera, Xilinx, PICCOLO as well as being great for SPI / IIC and test point access.

Tag-Connect’s TC2050-IDC has been selected as a Finalist in the Design News Best New Products of 2011 Golden Mousetrap Awards!

FEATURES & BENEFITS

◆ Zero Connector Cost per Board!
◆ Tiny Footprint!
◆ No mating connector required on your PCB!
◆ High-Reliability Spring-Pins for a Secure Connection!
◆ Save Cost & Space on Every Board!

TECHNICAL SPECS

◆ Available in 6, 10 and soon 20-pin “Legged” & “No Legs” versions.
◆ Legged version snaps to PCB for a prolonged secure connection. No-Legs version is hand-held during a quick programming operation.
◆ TC20x0-IDC cables terminate in standard ribbon connectors compatible with many device programmers. TC2030–MCP cables have RJ12 modular plugs to suite Microchip IDC3. -MINI-HDMI cables connect to Altium’s USB JTAG adaptor.

AVAILABILITY

Purchase now at Digikey, Mouser, MicrochipDirect, CCSinfo, Telexus.com, TheDebugStore, and others. See website for full details.

APPLICATION AREAS

MCU, DSP, FPGA & CPLD device programming and debug. Test Signal and ATE Access.
4 Channel 200 MHz 16-bit A/D with Virtex-7 FPGA VPX Onyx™ Board (Model 53760)

Supported FPGA/CPLDs: Virtex-7

Model 53760 is a member of the Onyx™ family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 53760 includes four A/Ds and four banks of memory. It features built-in support for PCI Express Gen. 3 over the 3U VPX backplane.

As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53760 to operate as a complete turnkey solution without the need to develop any FPGA IP. Users can install their own custom IP for data processing.

FEATURES & BENEFITS
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM

TECHNICAL SPECS
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Advanced reconfigurability features
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

APPLICATION AREAS
Aerospace/Defense, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications, Signal Intelligence, Software Radio, Radar

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**SAMC-713 High performance Virtex-6 AMC with VITA 57.1 expansion site**

**Supported Xilinx FPGA/CPLDs:** Virtex-6 LXT, Virtex-6 SXT

The SAMC-713 Advanced Mezzanine Card (AMC) is designed around Virtex-6 FPGA LXT and SXT families, combining great fabric flexibility and a colossal external memory benefiting from multiple high-pin-count, modular add-on FMC-based I/O cards.

The SAMC-713 is designed for applications requiring high performance, high bandwidth and low latency. The board takes full advantage of the Virtex-6 FPGAs power which makes the SAMC-713 perfect for reducing size, complexity and costs associated to leading-edge telecommunications, networking, data processing, industrial and medical applications. Moreover, FMC expansion site on the board offers almost unlimited I/O possibilities.

Combining Virtex-6 FPGAs LXT (up to VLX365T) or SXT (up to VSX475T) with four independent 2Gb DDRIII SDRAM memory banks and twelve high performance full-duplex GTX lines supporting Gigabit Ethernet, PCI express x1..x8 and Serial RapidIO x1..x4 The SAMC-713 gives OEMs an effective solution for wide range of applications. Scan Engineering Telecom also provides customization, turnkey integration and support to ensure that OEMs can focus where they prefer to add their own unique value.

**FEATURES & BENEFITS**

- Four independent 2Gb DDRIII SDRAM memory banks, total memory capacity 8Gb
- 12 full-duplex lines provides Gigabit Ethernet and PCI Express x1..x8 or Serial Rapid IO x1..x4 interfaces
- VITA 57.1 (FMC) expansion site, supports air cooled commercial and conduction cooled with region 1 form-factors with or w/o front panel
- Single Mid-Size or Single Full-Size AMC board

**APPLICATION AREAS**

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications, Other (please state below)

**TECHNICAL SPECS**

- Virtex-6 FPGA (from LX130T/195T/240T/365T to SX315T/475T), 20000-74400 Logic Slices, 9500-38300Kbit Block RAM, 480-2016 DSP48E1 Slices, up to 1000GMACS of processing power

**CONTACT INFORMATION**

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The XDSP-55 FPGA accelerator board is intended for high-performance SDR or data processing applications. The board also takes full advantage of the Virtex-4 FPGAs power, which makes the XDSP-55 perfect for telecommunications, networking, industrial, defense and medical applications based on CompactPCI form-factor and supports PCI 33/66MHz 32/64bit.

The XDSP-55 design is based on combined power of two Virtex-4 FPGAs which are operating as main FPGAs while service FPGA provides management and interconnection to the backplane. Using most powerful Virtex-4 FPGAs the board provides over 300000 logic cells or up to 1024 Xtreme DSP blocks while four ZBT SRAM memory banks connected to each main FPGA provides interconnect frequency up to 200MHz.

On top of this the XDSP-55 has reference quartz oscillator provides base frequency at 200MHz and frequency range from 10 to 550MHz. The board also has full-duplex LVDS channel for integration with other boards in CompactPCI chassis and speed over 800Mbit/s in each direction.

The XDSP-55 is intended for OEMs in telecommunications, data communications, industrial, defence & aerospace and medical markets.

**FEATURES & BENEFITS**

- CompactPCI form-factor, supports PCI 33/66MHz 32/64bit
- Two main FPGAs and one service FPGA from Xilinx Virtex-4 LX or SX families
- Four ZBT SRAM memory banks for each of main FPGA with high throughput
- Full-duplex LVDS channel, interconnection speed over 800Mbit/s in each direction
- Commercial (0...+50C) and industrial (-40..+85C) temperature range

**APPLICATION AREAS**

Aerospace/Defense, Broadcast, Data Processing and Storage, Industrial Automation, Wired Communications, Wireless Communications

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**AVAILABILITY**

Now

**TECHNICAL SPECS**

- Two main FPGAs, each can be Xilinx Virtex-4 (LX40- LX160 or SX55), for each FPGA: over 152000 logic cells (LX160), up to 512 Xtreme DSP blocks (SX55), up to 5760 kbit Block RAM (SX55)
- Four 72Mbit ZBT SRAM memory banks for each main FPGA, 72MB for total memory
- 256Mbit of nonvolatile Flash memory for main FPGAs configurations and 8Mbit of nonvolatile Xilinx PlatformFLASH memory for Service FPGA configuration
- Reference quartz oscillator with base frequency 200MHz, frequency range 10...550MHz and stability from 50ppm
- CompactPCI 3U 4HP board in commercial (0..+50C) or industrial (-40..+85C) temperature range
Spartan-6 FPGA Evaluation and Development Kits

Supported FPGA/CPLDs: Spartan-6 FPGA

Xilinx and Avnet provide a comprehensive offering of Spartan®-6 FPGA evaluation and development kits that enable designers to achieve an optimum balance of cost, power and performance.

The SP601 Evaluation Kit is a low-cost, entry-level environment for evaluating the Spartan-6 FPGA family with system design capabilities that include DDR2 memory control, flash, Ethernet, general-purpose I/O, and UART to name a few. The SP605 Evaluation Kit is a highly scalable base platform for developing low-cost applications requiring connectivity with high-speed serial transceivers, DDR3 memory control, DVI, parallel linear flash, and Tri-mode Ethernet.

The Xilinx Spartan-6 LX16 Evaluation Kit, featuring Texas Instruments battery management devices and power regulation circuitry and the Cypress PSoC® 3 Programmable System on Chip with embedded 8051 for an ultra-low-power controller. Avnet also offers the full-featured Xilinx Spartan-6 LX150T Development Kit for designing and verifying applications based on the Spartan-6 LXT FPGA family.

The low-cost Spartan®-6 FPGA LX9 MicroBoard is the perfect solution for designers interested in exploring the MicroBlaze™ soft processor or Spartan-6 FPGAs in general. The kit comes with several pre-built MicroBlaze “systems” allowing users to start software development just like any standard off-the-shelf microprocessor. The included Software Development Kit (SDK) provides a familiar Eclipse-based environment for writing and debugging code.

FEATURES & BENEFITS

◆ Xilinx SP601 and Avnet LX16 Evaluation Kits feature base board with Spartan-6 LX16 FPGA and ISE® WebPACK™ Design Suite (supporting Windows and Linux)
◆ Xilinx SP605 Evaluation Kit features base board with Spartan-6 LX45T FPGA and ISE Design Suite Logic Edition (device-locked)
◆ Avnet LX150T Development Kit features base board with Spartan-6 LX150T FPGA and ISE Design Suite Logic Edition (device-locked)
◆ The Spartan-6 LX-9 MicroBoard kit includes peripherals and expansion interfaces making it the kit ideal for a wide variety of applications. From a system running an RTOS to a Linux-based web server, the Spartan-6 LX9 MicroBoard can help you validate your next design idea.

Complete with universal power supply, accessory cables, and downloadable documentation with schematics, Gerber files, board BOM, and detailed user guides

TECHNICAL SPECS

◆ Xilinx SP601 Evaluation Kit for low-cost Spartan-6 FPGA evaluation and the Xilinx SP605 Evaluation Kit for low-cost connectivity applications
◆ Avnet LX16 Evaluation Kit for low-power, battery-power applications such as handheld data gathering, human machine interface, and embedded control
◆ Avnet LX150T Development Kit for PCI Express® bridges, Ethernet/Internet and video applications, and embedded controllers
◆ All kits feature industry-standard FPGA Mezzanine Card (FMC) connector enabling scaling and customization of base boards for specific application and market needs

AVAILABILITY

Available Today!

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications
VIRTEX-7 FPGA VC707 EVALUATION KIT

Supported FPGA/CPLDs: Virtex-7

The Xilinx Virtex®-7 VC707 FPGA Evaluation Kit provides a highly flexible base platform with an out of the box launch pad to evaluate and leverage designs that deliver breakthrough performance, capacity and power efficiency.

As a Base Level Targeted Design Platform, this kit provides a flexible environment for designs that need to implement a DDR3 memory interface, 10Gigabit Ethernet, PCI Express®, Analog Mixed Signal (AMS) capabilities, and other high-speed serial connectivity. Based on the Virtex-7 VX485T-2 FPGA, the kit is the optimal choice for advanced systems that need the highest performance and highest bandwidth connectivity, including advanced systems for wired and wireless communications, Aerospace and Defense, medical, and broadcasting markets.

The highly flexible kit combines fully integrated hardware, software and IP with pre-verified reference designs that maximize productivity and let designers immediately focus on their unique project requirements.

FEATURES & BENEFITS

◆ Virtex-7 FPGA family and 28nm leadership offering new benchmarks for performance and 50% power savings
◆ Faster start-up with integrated silicon, software, IP and complete documentation
◆ Rapid evaluations with Base Reference Designs and other pre-verified examples that exercise device and board features
◆ Convenient, easy-to-use GUI displays combine results from different implementations

TECHNICAL SPECS

◆ VC707 Base Board with Virtex-7 XC7VX485T-2FFG1761 FPGA
◆ Full Seat ISE® Design Suite Logic Edition device locked for the VX485T-2 FPGA
◆ Reference designs and demonstrations (please see Xilinx.com for latest designs) and board design files
◆ Documentation including a step-by-step Getting Started Guide
◆ USB Cables, Ethernet Cable, and universal power supply

AVAILABILITY

For more information about the Virtex-7 FPGA VC707 Evaluation Kit please visit www.xilinx.com/vc707

APPLICATION AREAS

Wired, Wireless, Aerospace and Defense, Medical, Broadcasting

CONTACT INFORMATION

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Xilinx Kintex-7 FPGA DSP Kit with High-Speed Analog

Supported FPGA/CPLDs: Kintex-7

In an industry where the need to deliver more performance and versatility is higher than ever, the Xilinx Kintex™-7 FPGA DSP Kit accelerates DSP designer productivity by allowing rapid migration to the 7 series device family, using a platform that fosters innovative and highly differentiated solutions.

The proven flexibility and industry leading price-performance of series FPGAs delivers more than 5000 GMACs of fixed-point and 1.3 TFLOPs floating-performance system performance, pushing the limits far beyond traditional DSPs in terms of total performance and performance per watt.

Each Xilinx DSP design platform provides out-of-the-box development solutions that streamline DSP development processes and improve productivity. The Kintex-7 FPGA DSP Kit includes development boards, IO daughter cards, design tools, and reference designs, and gives designers the industry’s largest portfolio of DSP, video, and floating-point IP blocks. Kit documentation shows how both RTL and high-level design methodologies can be used to extend and modify reference designs to end-user requirements.

FEATURES & BENEFITS

- Kintex-7 FPGA family and 28nm leadership drive up performance while slashing price and power
- High single-chip DSP performance
- Integrated Targeted Design Platform accelerates time to market with a combination of silicon, software, IP and reference designs
- Proven, easy to use design methods and high-level languages (MATLAB® and Simulink®) speed implementation and verification of DSP algorithms on FPGAs

TECHNICAL SPECS

- KC705 Base Board with Kintex-7 KX325T FF900 FPGA with full Seat ISE® Design Suite Logic Edition device locked for the KX325T FPGA
- 4DSP FMC150 High-Speed ADC/DAC FMC Module
- USB, Ethernet and MMCX RF coax cables, universal power supply, documentation, including Getting Started Guide
- Downloadable schematics, BOM, design files and targeted reference designs
- CoreGen IP and MathWorks® evaluation software (MATLAB and Simulink)

AVAILABILITY

For more information please visit www.xilinx.com/kintex7dsp

APPLICATION AREAS

Aerospace/Defense, Medical Imaging, Wireless Communications

CONTACT INFORMATION

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Delivering vital information on hardware, software, tools, services and solutions

www.eecatalog.com

A network dedicated to the needs of engineers, developers, designers and engineering managers
Synplify Premier - Fast, Reliable FPGA Implementation and Debug

Supported FPGAs/CPLDs: All the major FPGA/CPLD families of devices from Achronix, Microsemi, Altera, Lattice Semiconductor, Silicon Blue and Xilinx are supported.

As part of the Synopsys FPGA Design Solution, Synplify Premier software performs FPGA synthesis for programmable devices sold by Microsemi, Achronix, Altera, Lattice Semiconductor, SiliconBlue and Xilinx. The tool delivers the industry’s best Quality of Results (QoR), rapid runtimes using incremental synthesis, FAST synthesis mode and automated block-based design. Automatic compile-point technology automatically shortens synthesis runtimes by leveraging multi-core computers. Team-design features allow design team members to perform parallel and distributed development autonomously, further increasing efficiency. The Synplify Premier tool’s path-group technology makes design schedules more predictable by delivering results that are reproducible from one run to the next. The tool also delivers block-based RTL synthesis flows which fully integrate with 3rd party FPGA vendor block-based place and route design preservation flows, thereby shortening iteration runtimes, and preserving working, verified parts of the design from one run to the next.

For more information on Synplify Premier and other Synopsys FPGA implementation tools, visit us at www.synopsys.com/fpga

FEATURES & BENEFITS

◆ High reliability design for DO-254 compliance: Automatically implement safe FSMs and TMR insertion. Specify portions of the design to be preserved as debug logic or for deliberate redundancy purposes.
◆ Fast synthesis mode: Synthesize even the largest design in a fraction of the time required by other tools.
◆ DesignWare support: Easy ASIC code migration into an FPGA for prototyping. Integration with datapath and building block components in DesignWare IP.
◆ Automatic handling of DSP function: Infer DSP functions from RTL and map into vendor’s DSP hardware (e.g.: MACs, DSP48) for improved QoR.
◆ Team-design: Faster design iterations and design preservation. Develop a design in parallel and/or distributed environment using bottom-up or hybrid flow. No floorplanning required.

TECHNICAL SPECS

◆ Comprehensive language support including Verilog, VHDL, SystemVerilog and mixed-language.
◆ Supports Windows XP Pro and Windows 7 (32/64 bit).
◆ Supports Linux, RHEL4, RHEL5, and SLES9 (32/64 bit).
◆ Minimum hardware requirements: CPU 1 GHz speed or better, RAM 2Gb, HDD 300Mb free space.

AVAILABILITY

Synopsys’ Synplify Premier FPGA implementation software is available now. Request a free evaluation at www.synopsys.com/fpga

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications.

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www.eecatalog.com/fpga
Xilinx ISE Design Suite 13

Supported FPGA/CPLDs: Virtex Series, Kintex Series, Artix Series and Spartan Series and CoolRunner Family

ISE® Design Suite 13 maximizes productivity, by leveraging open industry standards to accelerate design creation, verification, implementation, and lower system power for design teams targeting Xilinx FPGAs. New to the award winning design tool and IP suite are enhancements which improve productivity across SoC design teams including the progression towards true plug-and-play IP.

Also new is an application called Documentation Navigator, allowing users to view and manage Xilinx design documentation (software, hardware, IP, and more) from one place, with easy-to-use download, search and notification features. To try out the new Documentation Navigator, now in open beta release, please visit www.xilinx.com/download today.

FEATURES & BENEFITS

◆ The new AMBA® 4 AXI-4 interconnect protocol IP enables design teams to easily customize their system topology for either performance or area resulting in optimal system bandwidth for interconnect and memory interfaces.

◆ Accelerated Verification: - Leveraging Xilinx’s large portfolio of development boards, kits and Xilinx’s ISE Simulator new hardware Co-Simulation, verification engineers can test implemented blocks of the design while leaving blocks under development in the simulator accelerating overall verification by up to 100 times faster than native simulation.

◆ Design Creation and Analysis – The PlanAhead™ Design and Analysis tool accelerates time to production with an integrated front-to-back environment with design analysis at each phase of the design cycle – RTL development, IP integration, verification, synthesis, place and route. The end result is rapid convergence on power consumption, resource utilization, and performance with fewer time-consuming design iterations.

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◆ Team Design – The new team design methodology addresses the challenge of multiple engineers working on a single project by providing a methodology for groups of developers to work in parallel.

◆ Enhanced Optimizations - Advanced optimizations, including intelligent clock gating that provides up to 30 percent dynamic power reduction, facilitates faster timing closure and timing preservation increasing overall productivity and reducing design iterations.

TECHNICAL SPECS

◆ ISE Design Suite Logic Edition: Front-to-back FPGA Logic Design with complete flow for RTL-based design

◆ ISE Design Suite DSP Edition: Complete design suite with DSP-specific IP and System Generator for rapid development of high performance DSP systems

◆ ISE Design Suite Embedded Edition: Integrated Embedded Design Solution supporting both embedded HW and SW engineers

◆ ISE Design Suite System Edition: Integrated tool and IP environment supporting the combined methodologies of logic/connectivity, embedded, and DSP design

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TRACE32-PowerTools - Category Embedded Development Tools


TRACE32 comprises a complete set of development and testing tools for the MicroBlaze, PowerPC PPC405, PPC440 and ARM Cortex processor IP. The modularity of TRACE32-PowerTools allows the user to extend the debugger with a trace extension and logic analyzer tools. The trace extension provides full support for program flow and data trace. In the context of FPGA systems, TRACE32-PowerTools enable the Xilinx ChipScope analyzer to access the target via the Lauterbach debug interface, in parallel with an ongoing debugging session. It also allows to configure the FPGA via the debugger and thus obviates the need for dedicated programming cables.

TRACE32 can be connected to the PC or workstation via USB or Ethernet, allowing for high-speed data transfer. Using Ethernet, it is possible to remotely use and share TRACE32 tools in a LAN of PCs and workstations. TRACE32-PowerTools are controlled by TRACE32-PowerView, a powerful IDE allowing HLL debugging on C or C++ level. It supports arbitrary third party compilers. TRACE32-PowerView allows unlimited software breakpoints and also supports the on-chip hardware break- and watchpoints. A fast FLASH programming utility is included. The comfortable graphical user interface is completely configurable by the user. It offers more flexibility than any other system.

FEATURES & BENEFITS

◆ Interface to all compilers for C/C++
◆ RTOS awareness
◆ FLASH programming utility
◆ Cache debugging and MMU support
◆ Trace extension up to 600 MHz and 4 GByte trace memory

TECHNICAL SPECS

◆ Download speed up to 5 MByte/s
◆ Powerful script language
◆ High-speed link via Ethernet or USB
◆ Universal hardware for all supported target architectures
◆ Display of internal and external peripheral registers at a logical level (peripheral browser)

AVAILABILITY

All products are available. More information can be found under http://www.lauterbach.com/pro_xilinx.html

APPLICATION AREAS

Aerospace/Defense, Automotive, Broadcast, Consumer, Data Processing and Storage, Industrial Automation, Medical Imaging, Wired Communications, Wireless Communications

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I predict that for many years into the future, semiconductor industry watchers will point to the 28nm process node as an era of vast semiconductor innovation and value led by FPGA vendors. At the 28nm node, FPGA vendors are taking pioneering steps into the world of 3D IC design by today shipping 2.5D stacked-silicon interconnect (SSI) FPGAs that shatter logic-capacity records and break Moore’s Law. At the same node, FPGA vendors are also broadening their markets to innovate an entirely new class of device called extensible processing platforms (EPPs)—processor-boot-first devices that will be attractive to software engineers, as well as hardware engineers. The 28nm node will also be seen as a time when a greater amount of analog functionality was integrated into FPGAs for new levels of system integration.

For over four decades, the semiconductor industry has been religiously following Moore’s Law, which holds that the transistor counts of devices will double every 22 months in lockstep with the introduction of each new silicon-process technology. All semiconductor vendors, especially FPGA vendors, have followed this law for decades.

28nm will go down as the node where FPGA vendors broke Moore’s Law. In the fall of 2011, Xilinx shipped a 28nm FPGA that has over two-million logic cell (equivalent to 20 million ASIC gates)—that’s over 2.5 times the capacity of the largest 40nm FPGA. We achieved this by implementing the device using 2.5D SSI technology, in which we place four FPGA slices (essentially FPGA dice) side-by-side on top of a passive silicon interposer. The passive interposer essentially functions like a PCB, facilitating the connections between the four die on the device (10,000 connections between each adjacent slice).

Many folks may view 2.5D as an intermittent step toward true, 3D IC, active-die-on-die stacking, but I predict 2.5D will prove to be a landmark technology in and of itself. For example, in the next 12 months, vendors will use this 2.5D SSI approach to field 28nm devices that place high-speed interconnect slices alongside FPGA slices on the same interposer, breaking bandwidth-records in addition to Moore’s Law. This SSI technology will allow semiconductor companies to offer innovative new devices and allow customers to achieve new levels of integration, reducing BOMs and lowering overall system power consumption. SSI Technology will be big.

In addition, at the 28nm node, vendors will begin to broaden their markets by introducing EPPs. For well over a decade, FPGA vendors have offered FPGAs with microprocessor cores pre-built into FPGAs or have offered soft microprocessors that users could implement in a given FPGA’s programmable logic. All these devices typically required users to program the FPGA to get the onboard processor to function. In this new class of device, the EPP, the processor boots first at startup. In fact, in the case of the Zynq-7000 from Xilinx, the device could be used as a standalone ARM processor and programmed out of the box by software designers who’ve never used or even heard of an FPGA. But the real value of such a device is that users will be able to make hardware and software tradeoffs quickly and offload functions to the programmable logic to achieve optimal system power and performance and innovative functionality for an untold number of applications.

Last but not least, the 28nm is facilitating the integration of more analog functionality onto FPGAs. Traditionally, most systems that incorporate an FPGA have required some degree of analog circuitry—A/D and D/A at a minimum—to allow the FPGA to communicate with other devices. Traditionally, this analog circuitry has been located on another chip. Having this circuitry now located on the FPGA improves performance, saves power and space requirements and reduces BOM—all increasing the value of the FPGA to the overall system.

The 28nm node is a landmark node for semiconductor innovation led by FPGA firms...you won’t forget it.

Vin Ratford is senior vice president of worldwide marketing, with responsibility for enabling sales to drive company revenue and profitability for Xilinx flagship programmable platforms, including silicon, design tools, methodologies, IP, boards and enabling technologies. Ratford joined Xilinx in 2006 when the company acquired Accelchip, where he served as president and chief executive officer.
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